UNIVERSITY OF THESSALY

MASTER'S THESIS

Design and Implementation of a Low Power Low Noise Operational Amplifier

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"Any sufficiently advanced technology is indistinguishable from magic."

Arthur C. Clarke

ΠΑΝΕΠΙΣΤΗΜΙΟ ΘΕΣΣΑΛΙΑΣ

Περίληψη

Τμήμα Ηλεκτρολόγων Μηχανικών και Μηχανικών Υπολογιστών

Διπλωματική Εργασία

Σχεδίαση και Υλοποίηση ενός Χαμηλού Θορύβου και Χαμηλής Κατανάλωσης Τελεστικού Ενισχυτή

Ευαγγελόπουλος Παναγιώτης

Για τους περισσότερους ανθρώπους η φράση "τεχνολογία του σήμερα" σημαίνει ένα πράγμα, ψηφιακή εποχή. Όμως οι περισσότερες ψηφιακές συσκευές δεν μπορούν να λειτουργήσουν χωρίς την βοήθεια των αναλογικών συσκευών. Επιπλέον, η ανάγκη για την δημιουργία ψηφιακών συσκευών χαμηλής κατανάλωσης έχει ωθήσει και την δημιουργία αναλογικών συσκευών χαμηλής κατανάλωσης. Η πιο συνηθισμένη και πολυχρηστική αναλογική συσκευή είναι ο Τελεστικός Ενισχυτής Δύο Σταδίων. Δυστυχώς, τέτοια κυκλώματα είναι επιρρεπή σε ηλεκτρονικό θόρυβο. Ο ηλεκτρονικός θόρυβος έχει παρόμοια συμπεριφορά με τον ακουστικό θόρυβο. Όταν είναι πολύ υψηλός, τότε η πληροφορία αλλοιώνεται και γίνεται λιγότερο χρηστική. Αυτή η εργασία στοχεύει στην δημιουργία ενός Τελεστικού Ενισχυτή χαμηλής κατανάλωσης με μικρά επίπεδα αυτοπαραγώμενου θορύβου χρησιμοποιώντας κορυφαία βιομηχανικά λογισμικά. Ξεκινώντας, θα μελετήσουμε την λειτουργία του Τελεστικού Ενισχυτή Δύο Σταδίων αναλύοντας τα υποκυκλώματά του και θα ερευνήσουμε τις μεθόδους δημιουργίας του ηλεκτρονικού θορύβου. Στην συνέχεια θα παρουσιάσουμε το λογισμικό που χρησιμοποιήθηκε καθώς και λεπτομερείς οδηγίες για τους νέους χρήστες. Συνεχίζοντας, θα βελτιώσουμε σιγά σιγά το σχέδιο με την βοήθεια των προσομοιώσεων μέχρι να ικανοποιεί τις δοσμένες προϋποθέσεις. Η προσεχτική επιλογή της τιμής των παραμέτρων θα καθορίσει τα αποτελέσματα να είναι επιθυμητά. Τέλος, όχι μόνο θα συνοψίσουμε τα αποτελέσματα και θα παρουσιάσουμε το τελικό σχέδιο αλλά επιπλέον θα συζητήσουμε και πιθανές μελλοντικές επεκτάσεις.

UNIVERSITY OF THESSALY

Abstract

Department of Electrical and Computer Engineering

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Design and Implementation of a Low Power Low Noise Operational Amplifier

by EVANGELOPOULOS Panagiotis

For most people, hearing the term "today's technology" one thing comes to mind; the digital era. But most digital devices can't function without the help of an analog device. Moreover, the need for low power digital devices grows day by day, and consequently so does the need for analog ones. The most common and versatile analog device is the Two-Stage Operational Amplifier. Unfortunately, analog devices are very susceptible to electrical noise. Electrical noise has the same effect as auditory noise. If the noise is too high then the information gets distorted and becomes less useful. This thesis aims to create such a low power analog device that also has low levels of self-inducing noise using industry-leading software. Initially, we investigate how a Two-Stage Operational Amplifier works by analyzing its sub-circuits as well as thoroughly examining noise generation and its types. Then, we present the software used along with some detailed instructions for new inexperienced users. Next, we slowly optimize the design to meet the given criteria through the use of simulations. Carefully selecting the value of each parameter will ensure desired results. Finally, we will not only summarize the findings and present the final design, but also discuss possible future work.

Acknowledgements

I would first like to thank my thesis advisor Professor Fotis Plessas not only for his guidance throughout the completion of this important educational task but also for his support during my entire academic career. He provided me with one-of-a-kind opportunities and he played a vital role in shaping my future path. I doubt I would be where I am today if it wasn't for him. I could never be more grateful.

Moreover, I would like to thank my friend and colleague Stavros Simoglou for setting up the server in which the software ran as well as for installing the software and writing the script files. He was eager to help whenever there was a problem with the software.

I would also like to acknowledge Professors Georgios Stamoulis and Christos Sotiriou as the readers of this thesis, and I am gratefully indebted for their valuable comments on this thesis.

Finally, I must express my profound and eternal gratitude to my family and friends for their unconditional love and support. I dedicate this thesis to my parents and brother, as a final gift, before I complete this chapter of my life and start the next. Without them, this monumental task would not have been possible.

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Chapter 1

Introduction

1.1 Thesis Purpose

The purpose of this thesis is twofold. Not only does it aim to analyze the inner workings of a Complementary Metal Oxide Semiconductor (CMOS) Operational Amplifier but also to learn the basics of an industry standard design software which will provide valuable experience for later work.

The design is based around the typical two stage CMOS Operational Amplifier. To avoid idealistic behaviour of the components, a library that contains models of real components has been used. This library is called SG13G2 and it is provided by Innovations for High Performance Microelectronics (IHP).

This design is focused around the following criteria:

- Two stage CMOS Operational Amplifier using the SG13G2 library at $130nm$.
- Powered by Single Supply source of $1.2V$.
- Output Open-Loop Gain of no less than $40dB$.
- Low Overall Power Consumption $< 20uW$.
- A Noise level of $5uV/\sqrt{Hz}$ @ $1kHz$ or less.
- Gain Margin of no less than $5dB$.
- Phase Margin of no less than 40°.

1.2 Chapter Overview

CHAPTER:2 presents a brief summary of the Operational Amplifier's history and then investigates the theory behind its operation. Noise is important in low noise design and thus it is extensively analyzed as well.

CHAPTER:3 introduces the software used and some of its most important capabilities. Step by step guides are available all the way from starting the program to running complex simulations.

CHAPTER:4 provides detailed explanations on how every component value was carefully selected though the analysis of simulation results.

CHAPTER:5 concludes with a summary of the results and presents the final design parameters of the two stage CMOS Operational Amplifier. It finalizes the thesis by proposing possible future optimizations.

Chapter 2

Theoretical Background

2.1 History

2.1.1 Defining Analog Signals

In this day and age everyone is familiar with the term *digital electronics* or *digital* in general but not everyone understands the concept of *analog electronics* which is the back-bone of today's modern miracles. So let's start by defining the term "analog" and explain its behaviour. The word is derived from for the Greek word ¨ανάλογος' (analogos) meaning "proportional" and this proportionality describes the relationship between a signal and a voltage or current that represents that signal.

But why are analog electronics so important? The answer lies in the nature of our universe. The world around us can not be described by variables that can take only two values. Things such as temperature, pressure, light intensity and sound can take any value possible which after being converted into electricity becomes a continual variable signal [1]. In contrast, digital systems lack this proportionality since they use only two discrete signal states *on* or *off* also known as *logic one* and *logic zero*. A somewhat crude example of the differences between the two types of signals is visible in FIGURE:2.1. Humans are by nature analog creatures and in order to "interface" with the digital world we need to take advantage of that property of analog systems.

2.1.2 History of Operational Amplifiers

There are many analog devices but this thesis focuses only on the Operational Amplifier (Op-Amp). The Operational Amplifier is a key component and a building block for many analog systems. Its invention started in the late 1920s at Bell Telephone Laboratories where the idea of a feedback amplifier was first conceived. That led to the creation of the first Op-Amp in 1941 which allowed for mechanical contraptions to be replaced

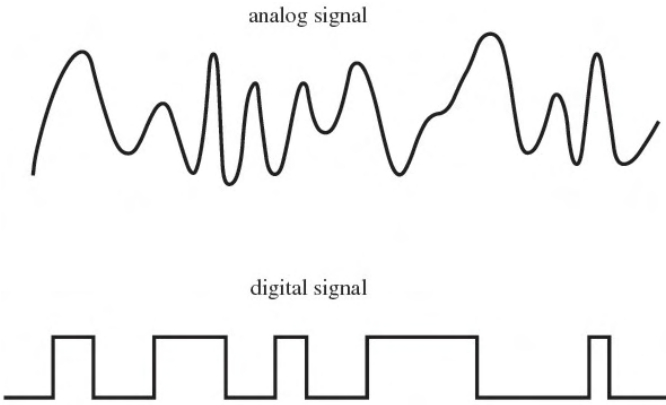


FIGURE 2.1: A comparison between an analog and a digital signal.

by silent and faster electronics. Early Operational Amplifiers were made with vacuum tubes and were used for early computers and military equipment (FIGURE:2.2a).

The invention of the transistor in the 1947 marked the beginning of the microelectronics era. Its importance became quickly apparent and alongside came the further development of the Operational Amplifier. Soon vacuum Op-Amps were replaced by transistor based Op-Amps. Those were modules, either on a Printed Circuit Board (PCB) or potted in resin, that were made with discrete components such as transistors, resistors and capacitors (FIGURE:2.2b).

Finally, in the mid 1960s the first Integrated Circuit (IC) Op-Amp was created which was a major transitional phase for Op-Amp history. Later, as the IC technology became increasingly more widespread in the latter half of the 20^{th} century, the Op-Amp became smaller and its production cheaper [2]. Since then Operational Amplifiers are continuously being expanded and optimized.

(A) GAP/R's model K2-W: A vacuum-tube op amp (1953).[3]

(B) GAP/R's model P45: A solid-state, discrete op amp (1961).[4]

FIGURE 2.2: Two types of early Operational Amplifiers.

2.2 Ideal Op-Amp and Theory of Operation

In this section the theory of operation of the Operational Amplifier will be analyzed. For simplicity and better understanding an ideal model will be used. To start with, the Op-Amp is a device that has two input terminals and one output terminal. The two input terminals are named Inverting Input and Non-Inverting Input and use the symbols "−" and "+" correspondingly. An ideal Op-Amp has some characteristics that are only valid in theory. There is a plethora of ideal characteristics but the most important ones are that the Operational Amplifier has an infinite open-loop gain ($G = \infty$), infinite input impedance ($R_{in} = \infty$) [5] and zero noise ($E_n = 0$). The last one interests us because noise is important in this thesis and thus it should be something we are familiar with.

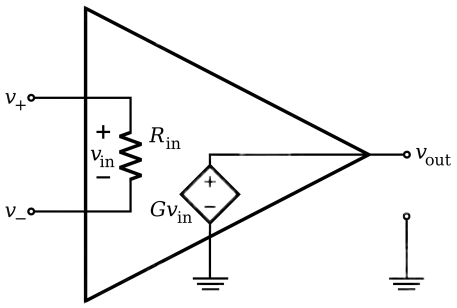


FIGURE 2.3: Inside an ideal Operational Amplifier.

In order to better understand how the Operational Amplifier functions, we shall take a look at the FIGURE:2.3 where the inside of an ideal Operational Amplifier is clearly visible. The two inputs are connected internally to the legs of the resistor R_{in}. Since this resistor is equal to infinity then, by Ohm's Law, the current that flows through the resistor is zero. And if the current is zero then the voltage drop across R_{in} is also zero. This allows v_{in} to be equal to the voltage difference at the input terminals ($v_{in} = v_+ - v_-$). The output, on the other hand, is not connected to any of the inputs directly. Instead, it is connected to a Voltage Controlled Voltage Source (VCVS) which is a type of dependant source. Here, the VCVS is controlled by the differential input voltage v_{in} that we described above which is also multiplied by a gain factor G. Now the output voltage can be calculated as seen in EQUATION:2.1.

$$v_{out} = Gv_{in} = G(v_+ - v_-) \tag{2.1}$$

Since $G = \infty$, it is obvious that any voltage difference at the input, no matter how small, will be amplified to infinity. Most of the time, this is not a desired behaviour so a limiting mechanism must be created. This mechanism is called *feedback* and its purpose is to attenuate the input based on the output. In order to understand this concept, a more detailed explanation is required. The FIGURE:2.4 shows an amplifier with a feedback loop. The input here is marked as S_i and the output S_o. In between there is a block named G, which is called *forward amplifier*, and a second block f, which is the *feedback network*.

If the feedback network is removed then the output is simply the input multiplied by the gain factor G which is basically the same as the Op-Amp configuration we saw in FIGURE:2.3. The gain when there is no feedback network, or $f = 0$, is called *open-loop gain* of the amplifier.

After the addition of the feedback network the output of the amplifier S_o is multiplied by a number f. If S_o and f have the same sign then S_{fb} gets subtracted from the input signal. This is called *negative feedback* and it is the most useful type of feedback. The gain when the feedback network exists is called *closed-loop gain*. So for the FIGURE:2.4 we have the following equation:

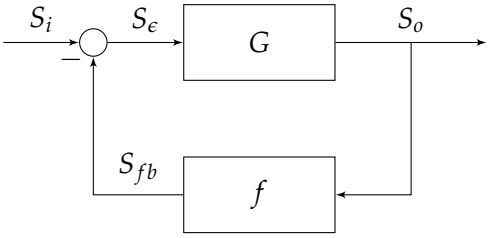


FIGURE 2.4: The diagram of a feedback amplifier.

$$S_o = GS_\epsilon = G(S_i - S_{fb}) = G(S_i - fS_o) \quad (2.2)$$

Solving for $\frac{S_o}{S_i}$ the closed-loop gain becomes:

$$G_{closed-loop} = \frac{S_o}{S_i} = \frac{G}{1+Gf} = \frac{1}{f}\left(\frac{Gf}{1+Gf}\right) \quad (2.3)$$

But this is an ideal Operational Amplifier and the gain is infinite, so we can assume $G_{fb} = Gf$ and take the following limit:

$$\lim_{G_{fb}\to\infty} G_{closed-loop} = \frac{1}{f} \quad (2.4)$$

Since the feedback network can be created just by using passive components, the value of f can easily be defined without the need to change any parameters of the active amplifier. This simplicity is what makes the Operational Amplifier such a powerful tool in analog electronics [5]. Moreover, by altering the value of f the Op-Amp can not only achieve simple tasks such as addition and subtraction of signals, but also more complicated non-linear tasks such as integration and differentiation. Those mathematical operations are where the Operational Amplifier got its name.

2.3 Noise and Noise Types

When explaining the ideal Op Amp one of the characteristics that was mentioned was *electrical noise*. Noise is a signal of unpredictable amplitude and frequency that can either be generated internally in the Operational Amplifier or superimposed by external sources. Its presence sets a lower bound where below it no input signals can be properly amplified. This is also often called *noise floor*. Unfortunately, in the real world it is impossible to completely eliminate electrical noise since its creation usually derives from the very nature of materials and from the movement of electrons inside them [6]. Understanding the different types of noise can help isolate the main contributor in a circuit and by further re-designing reduce its effects.

Noise is a random signal which means that it has instantaneous voltage spikes that can be either positive or negative in amplitude. Since that amplitude varies with time it can only be specified by a probability density function. The most common one is the

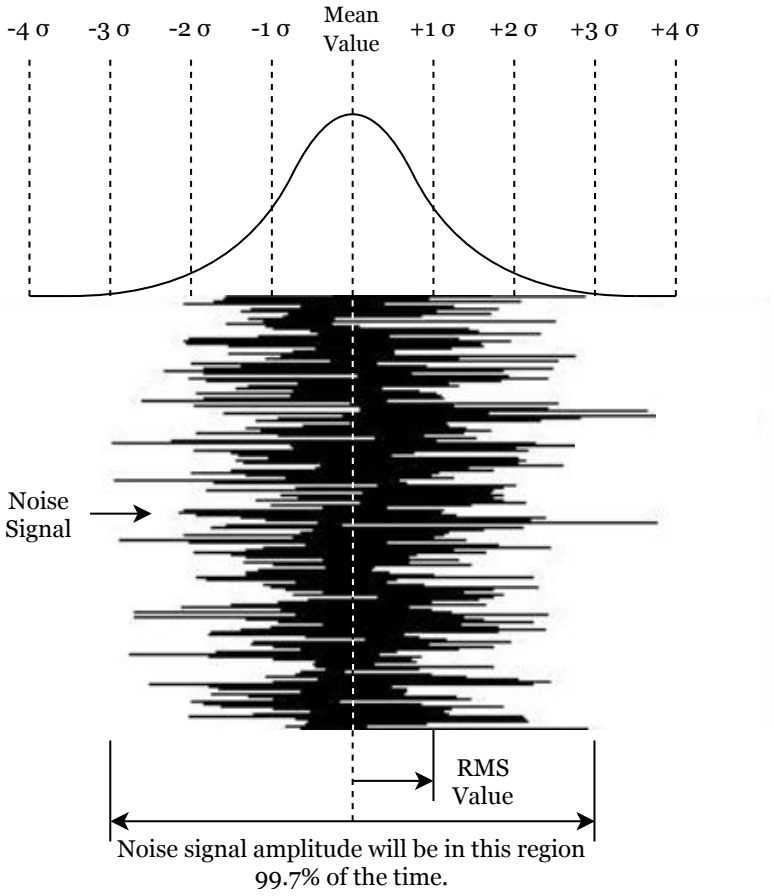


FIGURE 2.5: The Gaussian probability function for noise signals.

Gaussian and in such a probability function there is a mean value of amplitude that is

most likely to occur. The amplitude of noise can be theoretically infinite but as we can see from the FIGURE:2.5, it is quickly contained underneath the bell-shaped curve of the Gaussian distribution. The value σ is called standard deviation of the Gaussian distribution which is also the *rms* value of the noise signal. The amplitude of $\pm 1\sigma$ has an occurrence probability of 68%, $\pm 2\sigma$ has 95.4% and $\pm 3\sigma$ has 99.7%.

As all metrics, noise has its own units of measurement. It is normally specified as a spectral density in *rms* volts or amperes per root Hertz ($V/\sqrt{Hz}$ *or* $A/\sqrt{Hz}$). In order to acquire any useful information about the noise signal amplitude though, a frequency range and the gain are required. Below is an example on how to work with such units:

Assume an amplifier with a noise specification of $E_{noise}\ V/\sqrt{Hz}$ is used in a frequency range from f_{min} to f_{max} and with a gain factor of A.

- Calculate the bandwidth: $B = f_{max} - f_{min}$.
- Calculate the root Hz: $B_{root} = \sqrt{B}$.
- Multiply by the noise spec to get the equivalent input noise: $E_{in} = E_{noise} \cdot B_{root}$
- Multiply by the gain factor to get the output noise amplitude: $E_{out} = E_{in} \cdot A$

2.3.1 Shot Noise

Shot noise is caused by random fluctuations in the movement of electrons inside a conductor. When different types of conductors or semi-conductors, such as p-n junction, meet they can form a barrier. When electrons encounter such barrier, potential energy builds up until they have enough energy to cross that barrier (FIGURE:2.6). That sudden burst of energy released causes a tiny amount of noise and since there are a lot of electrons flowing in the system that noise can easily become pronounced [7].

The *rms* shot noise voltage is:

$$E_{sh} = kT\sqrt{\frac{2B}{qI_{DC}}} \tag{2.5}$$

Where:

k = Boltzmann's constant $1.38 \times 10^{-23} J/^{\circ}K$

q = Electron charge $1.6 \times 10^{-19} C$

T = Temperature in $^{\circ}K$

B = Bandwidth in Hz

I_{DC} = Average DC current in A

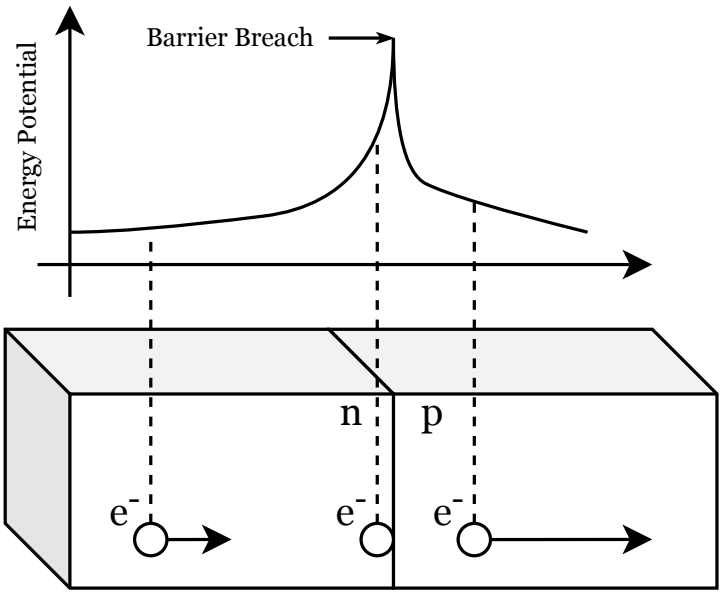


FIGURE 2.6: Shot noise of an electron breaking the barrier formed at a p-n junction.

Some of its characteristics:

- Associated with current flow
- Independent of temperature
- Spectrally flat

2.3.2 Burst Noise

Burst noise is yet another type of noise whose existence is heavily linked to the presence of heavy metal ions in the semiconductor material. This type is dependent on the manufacturing process and not on the design process and thus it is out of this thesis's scope.

2.3.3 Thermal Noise

Thermal noise is a bit more intuitive than shot noise. It is generated by the random movement of charged particles due to their thermal kinetic energy. As a result, it is obvious that thermal noise is linked to the temperature of the conductor. Higher temperature means more heat which in turn creates more random movement of the electrons which is finally interpreted as electrical noise (FIGURE:2.7). Usually thermal noise is more pronounced in resistors with higher values.

The *rms* thermal noise voltage is:

$$E_{th} = \sqrt{4kTRB} \tag{2.6}$$

Where:

k = Boltzmann's constant $1.38 \times 10^{-23} J/^{\circ}K$

T = Temperature in $^{\circ}K$

R = Resistance in Ω

B = Bandwidth in Hz

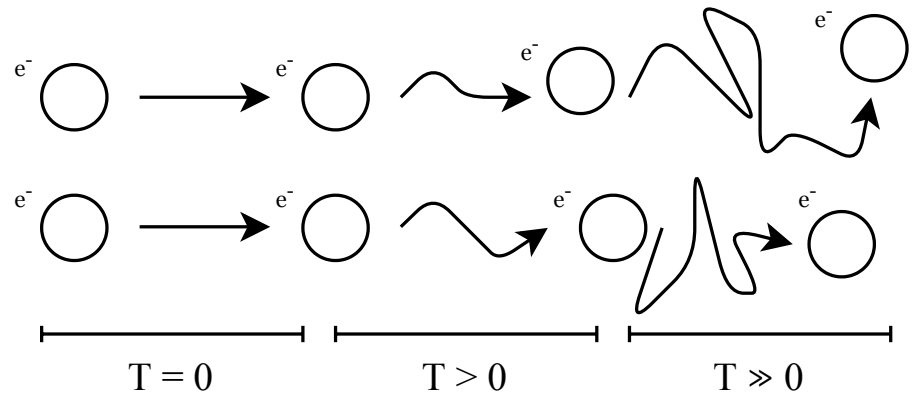


FIGURE 2.7: Electron movement based on absolute temperature.

Some of its characteristics:

- Highly dependent on temperature
- Noise stops at absolute zero
- Spectrally flat

2.3.4 Flicker Noise

Flicker noise is a type of noise that increases in amplitude as frequency decreases and for that reason it has a second name which is $1/f$ *noise*. It is present in almost all active and passive electronic components and it is rather difficult to reduce without any complicated techniques, such as *Chopping* and *Auto-Zeroing* [8]. Flicker noise is usually characterized by the $1/f$ *corner frequency* f_c which as seen in the FIGURE:2.8 can be approximated by finding the intersection of the two straight lines that best describe the two different type of noises [9].

Some of its characteristics:

- Increases as frequency decreases
- Associated with DC current

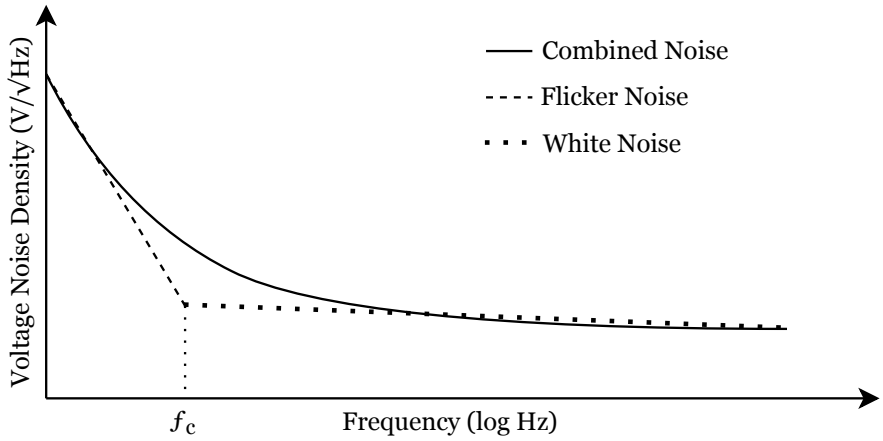


FIGURE 2.8: Approximation of the $1/f$ corner frequency.

Unsurprisingly, flicker noise will be present in the current design as well. Consequently, some alterations must be made to the design in order to meet the low noise requirement. Flicker noise is proportional to the DC current flowing through the circuit. Thus by keeping the power consumption low, the $1/f$ noise can also be kept under control.

2.3.5 Avalanche Noise

Avalanche noise is similar to shot noise but much more intense. It is created by reverse polarized p-n junctions and Zener diodes. If the electric field is intense enough the electrons will have enough energy to collide with atoms in the depletion region and create an electron-hole pair. This process is additive and generates large amounts of random current spikes that are interpreted as noise. This type of noise can be greatly reduced simply by avoiding the use of Zener diodes in the design.

The design in this thesis does not use any Zener diodes or reversed polarized p-n junctions, so the avalanche noise is minimal.

2.3.6 Noise Colors

Different types of noise can be categorized based on their spectral density. Spectral density is a metric which shows how the amplitude of noise signal changes depending on the frequency. The colors correspond to the power β of the frequency f^{β} to which their spectrum is proportional. TABLE:2.1 shows the different noise colors along with their corresponding frequency content and noise type. Note that the noise types mentioned in the sections above fall under the lower side of the color spectrum.

Color	**Frequency Content**	**Noise Type**
Violet	f^2	-
Blue	f	-
White	1	Thermal, Shot
Pink	$\frac{1}{f}$	Flicker
Red/Brown	$\frac{1}{f^2}$	Avalanche, Burst

TABLE 2.1: Noise colors and their frequency content.

2.4 Inside a CMOS Operational Amplifier

The circuit that is going to be presented is one of the most simple, common yet versatile schematics. Moreover, this circuit will be the foundation of this thesis's design. The circuit in FIGURE:2.9 is the one of a Two Stage Operational Amplifier. The name comes from the two discrete amplification stages of the design.

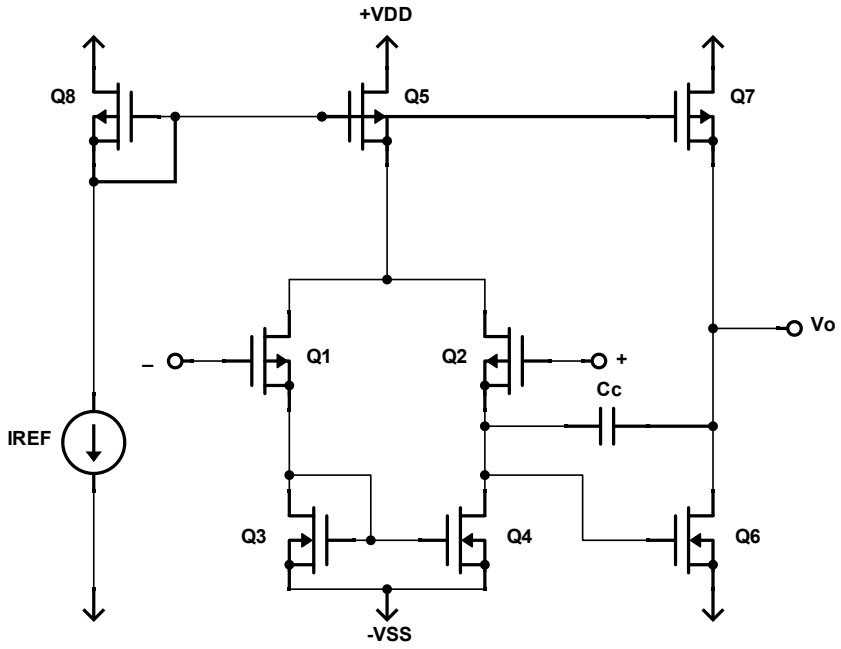


FIGURE 2.9: The two basic stages of a CMOS Operational Amplifier.

The circuit can be broken down into the following sub-circuits. The first sub-circuit is a differential amplifier with Q1 and Q2 being the differential pair and Q3 and Q4 forming a current mirror which acts as a load. This stage can have a gain factor of about $30dB$ while it also provides a fairly adequate Common Mode Rejection Ratio (CMRR). Next, there is the second stage which consists of the transistor Q6 forming a Common Source (CS) amplifier. Its input is the output of the previous stage and its output is the output of the Operational Amplifier. This stage can provide a gain of $35dB$ on its own and in combination with the first stage of the Op-Amp an overall theoretical gain of $50 - 60dB$ can be achieved. Finally, there is a third sub-circuit that provides the biasing current for the other two stages. The transistors Q8, Q5 and Q7 are part of a dual output current mirror which mirrors the reference current I_{REF} to the output of Q5 and Q7 [10]. Those power the differential amplifier and the CS amplifier respectively. The generation of such reference current I_{REF} is outside the scope of this thesis.

In order to understand the circuit better, a more in-depth explanation is required. Starting with the dual output current mirror, all PMOS transistors Q8, Q5 and Q7 function in the saturation region. So it is required that:

$$v_{DS} \leq v_{GS} - V_t \tag{2.7}$$

Where V_t is the threshold voltage of the PMOS. Moreover, in order to estimate the output current of the mirror, I_{Q5} and I_{Q7}, the following formula can be used:

$$\frac{I_{Q5}}{I_{REF}} = \frac{(W/L)_5}{(W/L)_8} \; and \; \frac{I_{Q7}}{I_{REF}} = \frac{(W/L)_7}{(W/L)_8} \tag{2.8}$$

Where W and L are the dimensions of the transistors. Keeping the dimensions the same for all three transistors will force the Mirror Ratio (MR) to be 1 and the currents to be equal.

For the differential amplifier the voltage difference between the drains of the two PMOS transistors Q1 and Q2 should be zero when the gates of those transistors are grounded. Any miss-matching in the transistor dimensions or difference in the biasing current will cause the voltage difference to shift away from zero. To avoid this, perfect matching between Q1 and Q2 is required. This is achieved by keeping the following equation true:

$$(W/L)_1 = (W/L)_2 \tag{2.9}$$

For the Q3-Q4 mirror we follow almost the same reasoning. Assuming the current that flows through Q2 is $I_{Q2} = I_{REF}/2$, we can then take Kirchhoff's Current Law (KCL) to find the current I_{Q4}.

$$I_{Q2} - I_{Q4} - I_{C_c} - I_{GATE_{Q6}} = 0 \tag{2.10}$$

But in theory, the input impedance of the Q6 NMOS is infinite and thus no current is flowing into the gate. Similarly, no current flows through the compensation capacitor C_c. So $I_{GATE_{Q6}} = 0$ and $I_{C_c} = 0$ and from the EQUATION:2.10 we get:

$$I_{Q3} = I_{Q4} \tag{2.11}$$

That means that the current mirror that acts as a load to the differential pair has a $MR = 1$ which can be broken down to:

$$MR = \frac{I_{Q3}}{I_{Q4}} = \frac{(W/L)_3}{(W/L)_4} = 1 \Leftrightarrow (W/L)_3 = (W/L)_4 \tag{2.12}$$

The only component that has not been analysed yet, is the Compensation Capacitor

C_c, also known as Miller capacitor. In order to stabilize the Operational Amplifier at high frequencies, a capacitor is placed across the high-gain stage. This places the poles on the Left-Half Plane (LHP), but due to a feed-forward path, it also adds zeros to the Right-Half Plane (RHP). This addition of zeros degrades the phase margin. In [11] a comprehensive guide is presented to help with this problem. A resistor is added in series with the Miller capacitor in order to move everything to the left and keep the RHP empty. This will be easily visualized during the simulation process in SECTION:4.2.5.

Chapter 3

Software

3.1 About Cadence® Virtuoso®

Another important aspect of this thesis is to gain experience using an industry standard tool for analog development. For this purpose the industry-leading platform Cadence® Virtuoso® was used. It supports custom analog, digital, and mixed-signal designs at the device, cell, block, and chip levels. Moreover, the Virtuoso Schematic Editor, the Virtuoso Analog Design Environment and the Virtuoso Layout Suit enable the creation of custom designs that are both fast and silicon accurate.

3.1.1 Tool Libraries

For the completion of this low power and low noise operational amplifier two libraries were used. The first one is *analoglib* by Keysight Technologies which provides a handful of useful ideal components as seen in this [12] catalogue. For this design ideal voltage and current sources were used so that the noise would be entirely generated by the internals of the Operational Amplifier. This provides a more precise noise profile and consequently accurate measurements.

The second and most important library is the *SG13G2* library provided by Innovations for High Performance Microelectronics (IHP). It is based on the SiGe:C BiCMOS technology at $130nm$ with $3.3V$ and $1.2V$ logic CMOS voltages of which the latter was used. Unlike the *analoglib* mentioned above, the *SG13G2* library has its components modeled from the actual fabricated components. This enables the simulation to be as realistic as possible. Some key specifications for this library can be seen in TABLE:3.1.

3.1.2 Simulation Engines

The Virtuoso platform is compatible with a variety of different simulation engines. One of them is the "Simulation Program with Integrated Circuit Emphasis" or *SPICE*

Feature	SG13G2
Technology node (nm)	130
CMOS core supply (V)	1.2, 3.3
C_{MIM} ($fF/\mu m^2$)	1.5
Poly Res ($\Omega/\square$)	275
High Poly Res ($\Omega/\square$)	1360

TABLE 3.1: Some key specifications of the SG13G2 library form IHP [13].

which is an open-source simulation engine that is widespread and commonly used. However, the Spectre® Platform was used instead. It is developed by Cadance and its optimizations and accuracy marked it as one of industry's best solutions for analog simulations.

3.2 Getting Started

In this section a few basic steps will be presented not only for setting up, creating and executing project files, but also for creating libraries, schematics and simulations. This will not be a detailed step-by-step guide since the documentation for this software is well written. However, it will provide some basic information for anyone who wants to make a quick start.

3.2.1 Bash Scripts

The software runs on CentOS 7, one of many Linux distributions, which is highly reliable and stable, making it suitable for enterprise workloads. A *bash* script is a plain text file which contains a series of commands. These can all be executed by simply running the script file. This provides an effortless way to start-up Virtuoso.

First, a new directory must be created inside the `/home` path. For example, let's assume a new folder with the name `project` is created. Now, two bash scripts must be created inside `/home/project`. The first one will be called `"create_project.sh"` and will have the following commands inside:

```
1 #!/bin/bash
2
3 PROJECTPATH=$1
4
5 mkdir -p $PROJECTPATH
6
7 cd $PROJECTPATH
```

```
8
9  PROJECTPATH=$(pwd)
10
11 cp /home/PDK/IHP_SG13G2/Cadence/SG13G2_617_rev1.0.1/work/skel/* ./
       -R
12
13 SEDPATH=$(echo $PROJECTPATH | sed 's_/_\\/_g')
14
15 sed -i  "s/setenv\ PROJECT\ ???/setenv\ PROJECT\ $SEDPATH/g" ./cds/
       cshrc.cadence
16
17 cd ./cds
```

And a second one called "exec_project.sh" with the following commands:

```
1  #!/bin/bash
2
3  pushd .
4  EXECPROJECT=$1
5
6  cd $EXECPROJECT
7
8  cd cds
9  csh <<< "source cshrc.cadence; setenv OA_UNSUPPORTED_PLAT
       linux_rhel60; virtuoso"
10
11 popd
```

In order to create a project folder with the name "PROJECTPATH" this command:

```
./create_project.sh PROJECTPATH
```

must be executed in the project directory through the console. After it is done, a folder will have been created inside /home/project that contains all the appropriate files for Virtuoso to run. This process only needs to be done once. After that, in order to launch Virtuoso the command:

```
./exec_project.sh PROJECTPATH
```

needs to be executed in the same console window.

3.2.2 Creating a Library

After the execution of the last script mentioned in the previous section, two windows should appear on the screen. One is the **Virtuoso Log** where information about errors and

warnings during the designing and simulation are shown, and the other is the **Library Manager** where new custom libraries and cells can be created. For analog designs, two libraries should be already loaded. As mentioned in a previous section, the *Cadence_IC* library contains some basic and ideal components and the *SG13G2* is provided by IHP, which contains accurate models of components and their layout scheme.

In order not to alter these important libraries, a new one should be created that will contain all the cells of the project. Let's create a new project, for example, a simple voltage divider.

In the **Library Manager** window go to `File > New > Library...` and proceed to name the custom library without changing the directory. Afterwards, a window called **Technology File for New Library** will show. Select the bullet *"Attach to an existing technology library"* and click `OK`. Select the *SG13_dev* library and click `OK`. Now the groundwork has been laid and the creation of a new cell can begin.

3.2.3 Creating a Cell

A cell can either be a custom component used in a complex circuit or just a simple project. Here, two new schematic cells will be created in order to later explain the different types of simulation.

FIGURE 3.1: The "New File" window during the creation of a new cell.

First, select the new library from the menu on the left in the **Library Manager** and then create a new cell by going to `File > New > Cell View...` . In the **New File** window type a name for the cell and set the rest of the parameters as seen in FIGURE:3.1. After clicking `OK`, do the same for the second cell with the name *"low_pass_filter"*.

3.2.4 Schematic Editor

By simply clicking on one of the cells in the **Library Manager** window, the **Virtuoso® Schematic Editor L** window automatically launches. This is the editor where the circuit is going to be created.

Some of the most useful actions and sortcuts can be viewed in TABLE:3.2 but an even more detailed guide can be viewed by going to `Help > Schematics User Guide`. It is worth mentioning that the documentation is very well written with detailed explanations and should be consulted whenever questions arise.

Key / ShortCut	**Action**
F	Fit to screen
I	Add instance
W	Add wire
R	Rotate
C or Shift+Drag	Copy
Ctrl+Drag	Move component without the wires
Q	Edit component properties
L	Label wire
ESC	Deselect
U	Undo
X	Check Schematic
Shift+X	Check and Save[1]
Shift+MouseWheel	Zoom
MiddleMouseClick	Pan

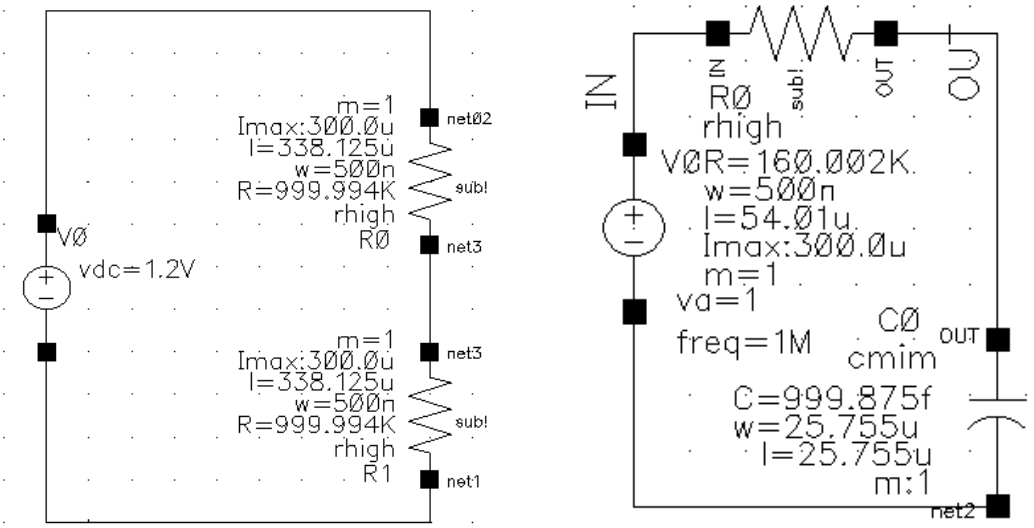
TABLE 3.2: Most useful shortcuts. More can be found in [14].

Now to create a simple voltage divider, open the **Add Instance** window by pressing `"I"`. From the Library drop-down menu select *SG13_dev*, from the Cell select *rhigh*, tweak the parameters to your liking and click the button `Hide`. Place the resistor by left-clicking on the schematic canvas and press `"ESC"` to stop adding components. Now to add a voltage source press `"I"` and select the *analogLib* from the Library drop-down menu. Ideal components can be found inside this library as well. From the Cell, select *vdc* and in the field *"DC Voltage"* enter the desired voltage. By pressing `"Shift+X"` the editor checks the schematic for any errors and warnings and then saves the file. FIGURE:3.2a shows the circuit made.

By following a similar set of steps, the low pass filter schematic was easily created (FIGURE:3.2b) in its own cell view. Here, an AC source was used by selecting the cell *vsin*

[1] No "Undo" actions can be done after a "Check and Save" action!

from the *analogLib* library. Both fields *"AC magnitude"* and *"Amplitude"* are filled with the value of $1V$ and in the *"Frequency"* field $1MHz$ is put. The capacitor's cell name in the *SG13_dev* library is *"cmim"*. After placing the wires, the `"L"` key was used to label them. This is done so they can be referenced and used later in the simulation.



(A) Voltage divider circuit.

(B) Low-pass filter circuit.

FIGURE 3.2: Two test circuits in Virtuoso Schematic Editor L.

3.2.5 Simulation Types

In order to extract information from the schematic that has been created, a simulation needs to be run. Virtuoso has the **ADE L** program, which is a simulator interface that runs Spectre in its core. **ADE L** can be started by going to `Launch > ADE L`. The *"Design Variables"* sub-window will show all available variables that are present in the design. To create such a variable, insert a name instead of a value in the component field you wish to vary. For example, to create a resistor with a variable resistance, insert a name like *r_var* into the *"R"* field in the resistor properties menu. If the variable does not show immediately in the *"Design Variables"* sub-window, right-click and select the option `"Copy From Cellview..."`. Variables like these are especially useful when doing parametric simulations (SUBSECTION:3.2.5.4).

The state of the **ADE L** program can be saved by going to `Session > Save State...`, choosing a name for the state and then clicking `OK`. In similar fashion, a state can be loaded into **ADE L** by going to `Session > Load State...`.

An important note is to remember to always check and save before running a simulation or else it will not work properly.

3.2.5.1 DC Analysis

The DC analysis is done to view the DC operating points of the schematic. It is a very useful simulation that should always be enabled. To create a DC analysis go to `Analyses > Choose...` and in the window that popped up select the *"dc"* bullet. Afterwards, check the *"Save DC Operating Point"* box and before clicking `OK` make sure the *"Enabled"* box is also checked. Now the DC analysis can be seen in the *"Analyses"* sub-window.

By going to `Simulation > Netlist and Run` the simulation can be started. On the bottom right of the **ADE L** window a status bar will show the progress of the ongoing simulation. When ready, an appropriate message will be shown.

To view the results of the DC simulation go to `Results>Annotate>DC Node Voltages`. This will annotate the voltage and current values of each node directly onto the schematic. Below is the voltage divider example from earlier with the annotated voltages.

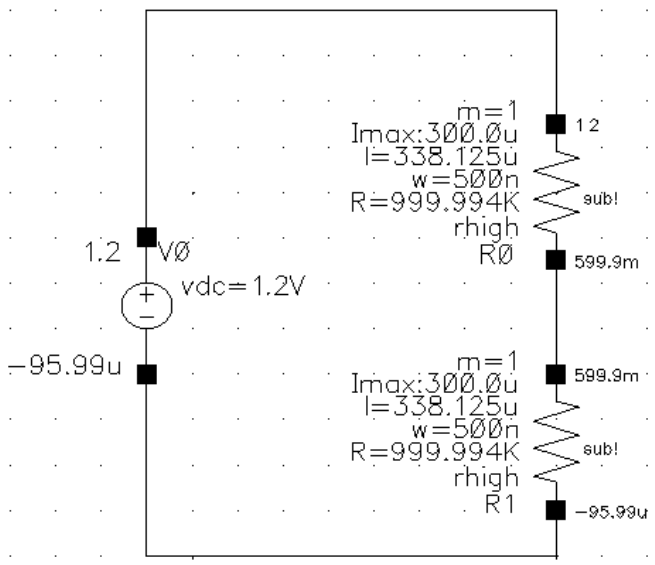


FIGURE 3.3: The voltage divider example with annotated voltage values after the simulation.

3.2.5.2 Transient Analysis

The transient analysis is done when there is a need to plot a signal against time. To initiate such analysis, choose the *"tran"* analysis, enter in the *"Stop Time"* field the time at which the simulation stops and check the *"Enabled"* box before clicking `OK`. Everything else should be left at default values for simple simulations.

After the simulation is run, the signal can be plotted by going to `Results > Direct Plot > Main Form...` For the low-pass filter example we mentioned above, the *"Voltage"* function is selected first and then the *"Add To Outputs"* box is checked in order automatically run this plot every time the simulation is run. Finally, instead of clicking `OK`, click on the net you wish to plot. In this example, we want to plot the nets *"IN"* and *"OUT"* so the procedure described above is done twice. Below is a view of the **ADE L** window (FIGURE:3.4) and the plotted signals (FIGURE:3.5).

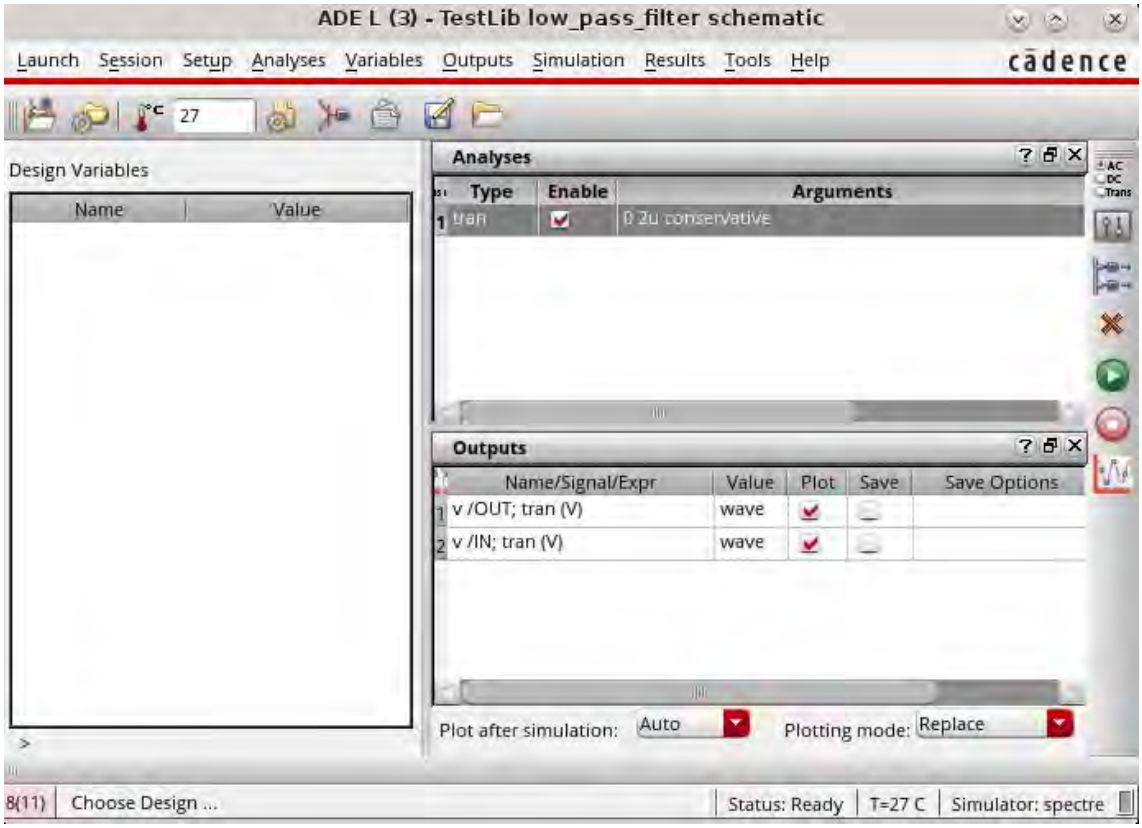


FIGURE 3.4: ADE L window.

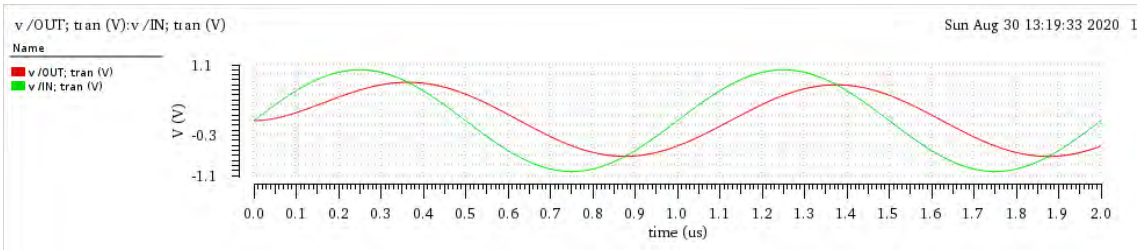


FIGURE 3.5: Input and output plots of the low-pass filter.

3.2.5.3 AC Analysis

The AC analysis is done when wanted signals need to be plotted against the frequency domain. This time the *"ac"* bullet is selected with the frequency being the sweep variable. In the *"Sweep Range"* sub-window the *"Start-Stop"* bullet is selected. For this example we will run the filter from $10Hz$ to $100MHz$. The *"Sweep Mode"* is set to *"Automatic"* and the *"Enabled"* box is once again checked before clicking `OK`.

To view the frequency response of the low-pass filter, we go to `Results > Direct Plot > Main Form...`, select *"Voltage"* and the *"OUT"* net on the schematic with the *"dB20"* modifier, add it to the outputs and, finally, plot it. For the phase response the same steps are taken but the *"Phase"* modifier is selected instead. FIGURE:3.6 shows the plots generated. From them it can easily be deduced that the cut-off frequency of the filter is around $1MHz$.

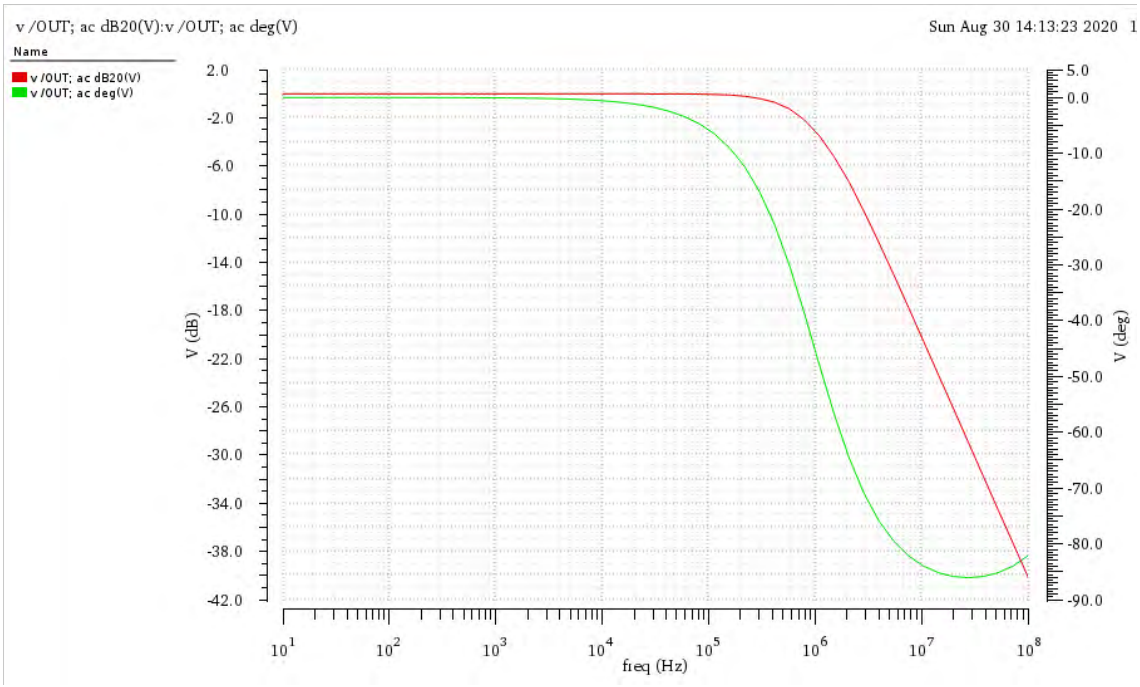


FIGURE 3.6: Frequency and Phase response of the low-pass filter.

3.2.5.4 Parametric Analysis

The parametric simulation is one of the most important things when creating complicated schematics. Its usefulness becomes apparent when there is a need to see how the signals change based on the different values of a component parameter. Let's assume that we would like to view how the frequency response of the filter changes as the value

of the capacitor changes. First, the properties window of the capacitor is opened by selecting the capacitor and then pressing the `"Q"` key. At the *"C"* field the variable name *"cvar"* is inserted before clicking `OK`. Afterwards, `"Shift+X"` is pressed to check and save the schematic. Now at the **ADE L** window we right-click in the *"Design Variables"* and select *"Copy From Cellview..."*. The variable appears on the list and a default value of $1p$ is inserted. With the *"ac"* analysis enabled we go to `Tools > Parametric Analysis...` and double-click on the *"Add Variable..."* field to add the variable we created. For this example, the capacitor is going to vary from $0pF$ to $10pF$ with a step size of $1pF$. In order to do that, check the *"Sweep?"* box to enable the sweeping of this variable and proceed to fill the *"From"* and *"To"* fields. The *"Step Mode"* is set to *"Linear Steps"* and the *"Step Size"* is set to $1p$. Finally, the green play button on the **Parametric Analysis** window is pressed and the parametric analysis produces the plots below.

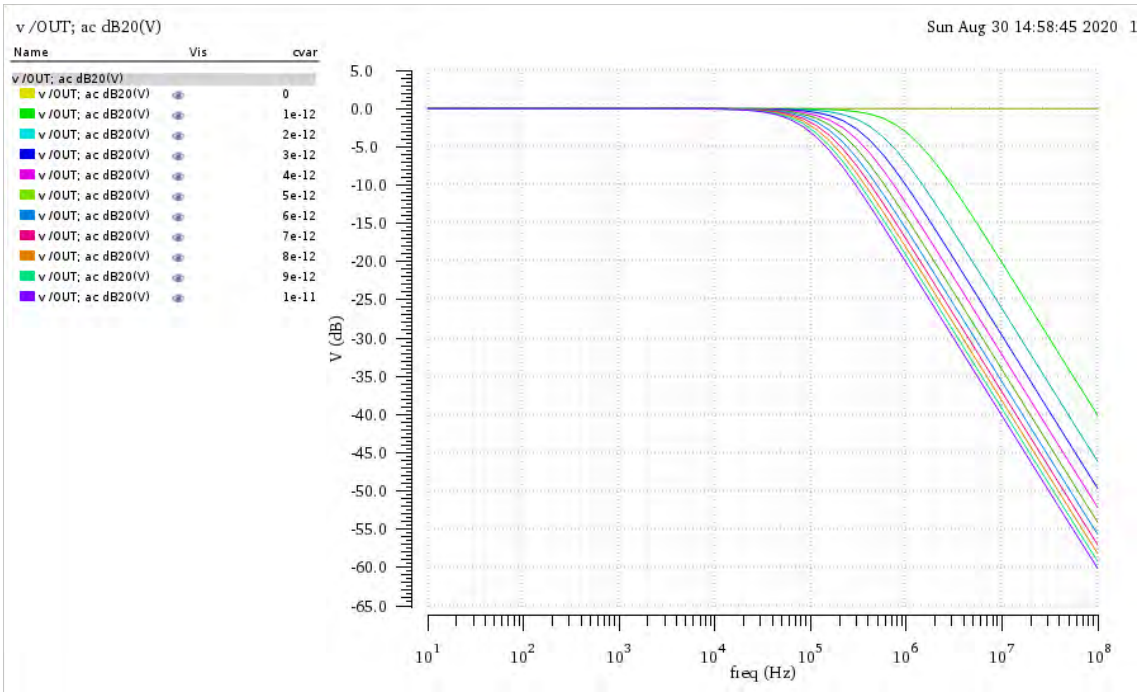


FIGURE 3.7: Frequency response of the low-pass filter for different capacitor values.

Parametric sweeps can be saved and loaded for easy use and multiple variables can be added by right-clicking and selecting `Insert Row`.

Chapter 4

Design and Simulations

By combining the information gained from the previous two chapters, the design of the Two Stage CMOS Operational Amplifier can finally begin. Mathematical formulas were only used as a guide during the initial designing procedure. Fine tuning of the component parameters was done through extensive parametric simulation testing and careful evaluation of the simulation results.

4.1 Initial Design

The design of this Low Power Two Stage CMOS Operational Amplifier is heavily based on the design shown in FIGURE:2.9 which was analyzed in SECTION:2.4. An initial design identical to the one in FIGURE:2.9 was first created to provide a basic building block from which we can later expand upon. In FIGURE:4.1 the initial design can be seen along with the voltages of each node.

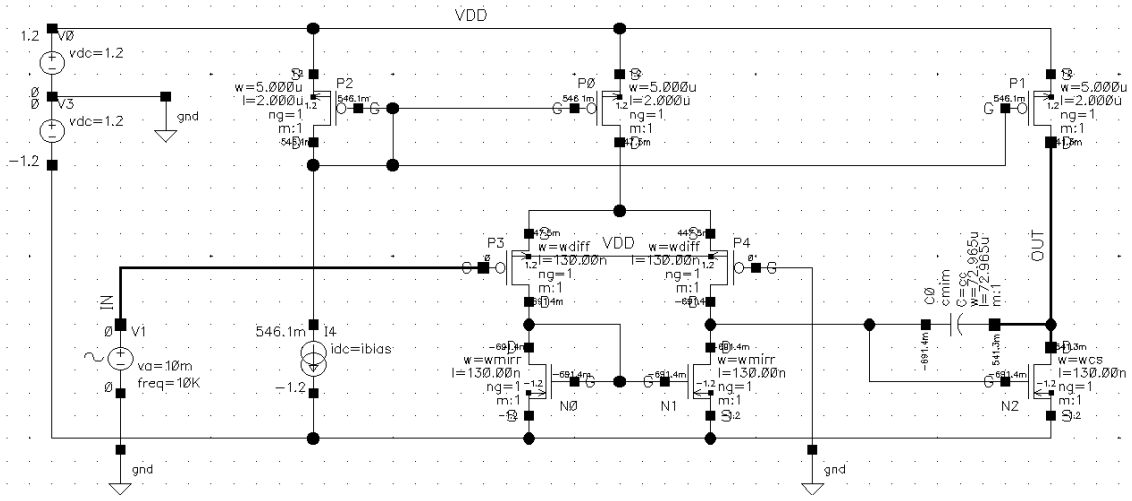


FIGURE 4.1: The initial design of the CMOS Operational Amplifier.

However, the specifications call for a single supply design. Negative voltage power rails are uncommon in many recent designs and are often difficult to produce. Thus, single supply Operation Amplifiers are preferred. Switching from a dual to a single supply can not be done without altering the schematic. Eliminating the negative rail will greatly affect the DC biasing currents and voltages of the CMOS transistors which will change their operating regions and will ultimately render the Operational Amplifier unusable.

To fix the biasing problem, a voltage source needs to be placed in series with the gates of the differential pair transistors. This will allow the transistors to operate in the saturation region. Those voltage sources are not part of the internal design of the Operational Amplifier but rather a part of the input signal itself. Usually, that is considered problematic and a DC blocking capacitor is placed in the path of such signals to remove any DC offset. However, since this design is not an individually self-contained Operational Amplifier but is a part of a bigger, more complex design, it is safe to assume that input signals as well as output signals are going to have that DC offset. The reason for such an assumption is that DC blocking capacitors are physically many times larger than the circuit itself when laid out on silicon and in order to keep the design as small as possible their usage is avoided.

The input DC offset is not the only input to the circuit that is generated by external means. The reference current for the dual output current mirror is also generated externally. Even though the design of a current source is outside the scope of this thesis, some useful information can be found in [15] and [16].

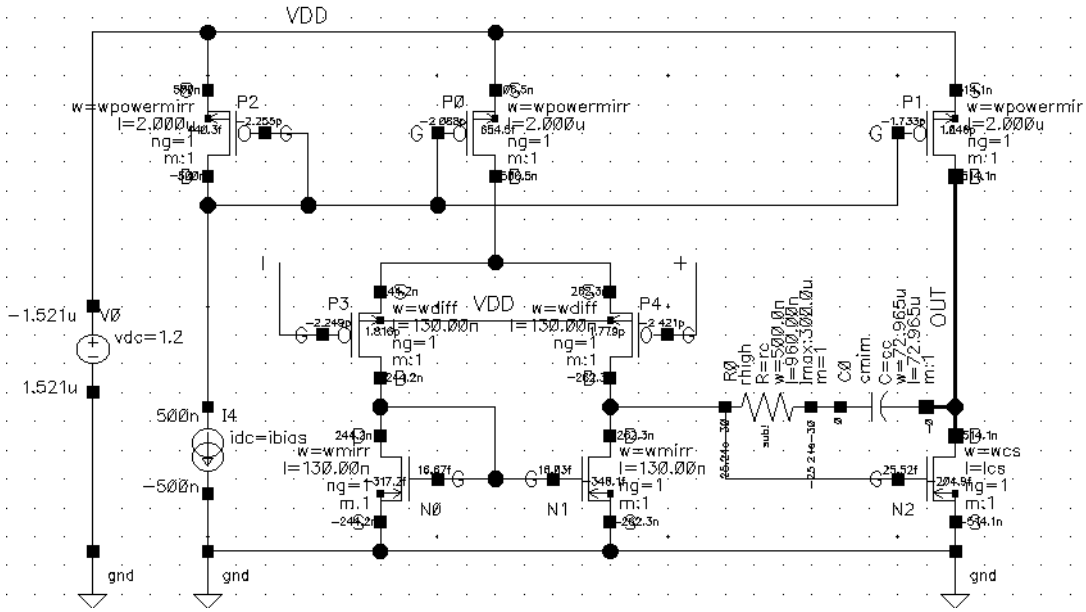


FIGURE 4.2: The final design of the CMOS Operational Amplifier.

The single supply design is visible in FIGURE:4.2. Any input signal circuitry is not shown here but is shown in figure FIGURE:4.3 instead.

4.2 Simulations

The simulation phase is extremely important for determining the component parameters that allow the Operational Amplifier to function properly. A parametric analysis that varies all parameters at the same time would surely give off the best possible combination but it would also take a tremendous amount of computing power and time which are not available. So smaller separate parametric simulations were ran instead.

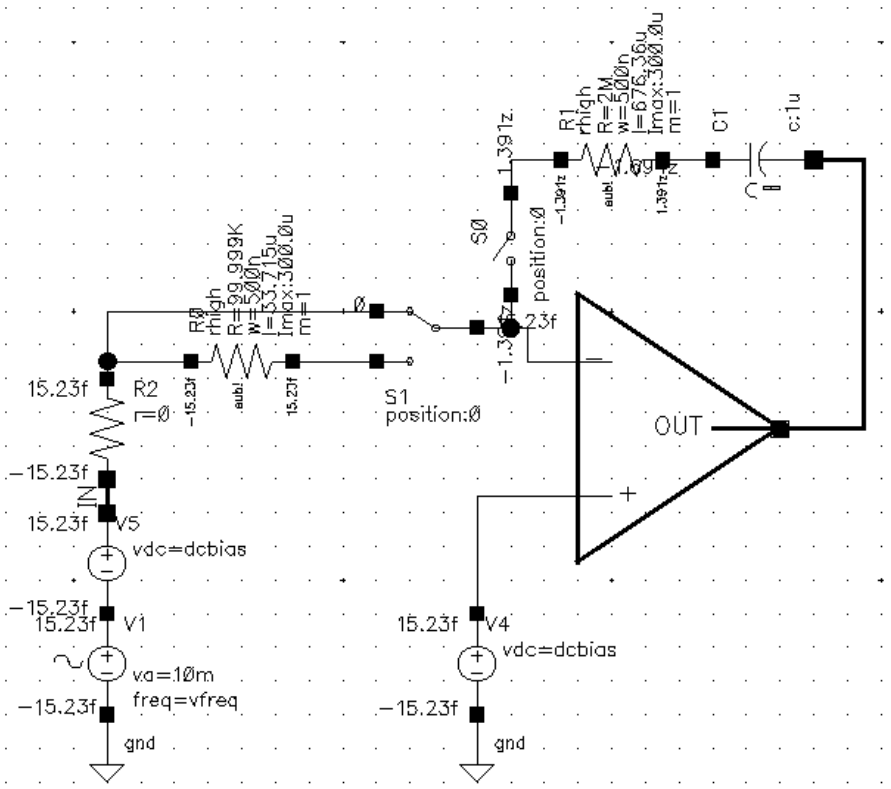


FIGURE 4.3: The testing circuitry for the simulations.

FIGURE:4.3 shows the external testing circuitry of the Operational Amplifier. Most of the simulations will run using this setup. The whole amplifier shown in FIGURE:4.2 is represented here by the classic triangular symbol of the Operational Amplifier. The source $V1$ is the signal source and the sources $V4$ and $V5$ are the ones representing the input DC offset that was mentioned in SECTION:4.1. The rest of the circuit is a simple way of changing between open-loop and closed-loop configurations without having to alter the main schematic.

4.2.1 Differential Amplifier

As instructed, the length of the PMOS transistors that form the differential pair is maintained at $130nm$. In result to this, only the width of the transistors can be altered. The FIGURE:4.4 shows how the output open-loop gain of the Operational Amplifier changes depending on the width ($wdiff$) of the two transistors.

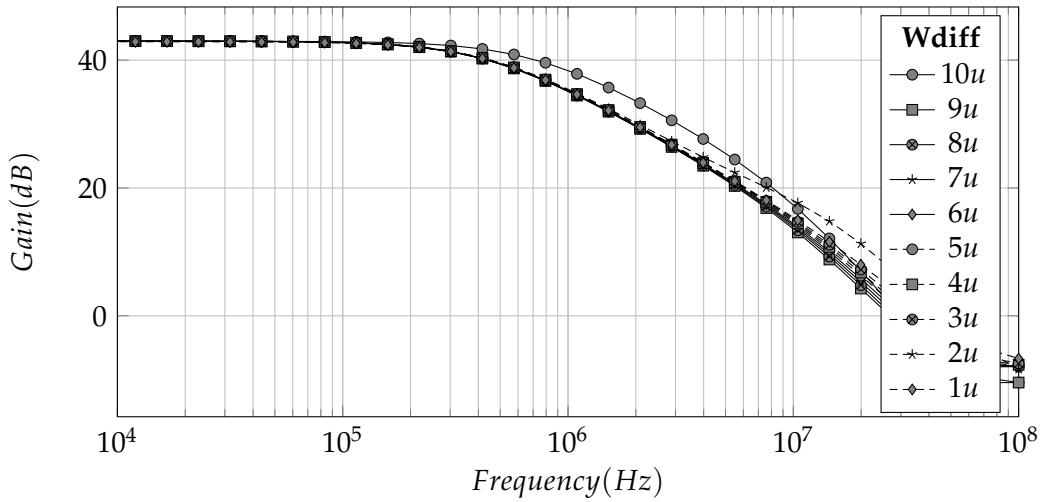


FIGURE 4.4: Open-loop Gain dependence on the differential pair transistor width.

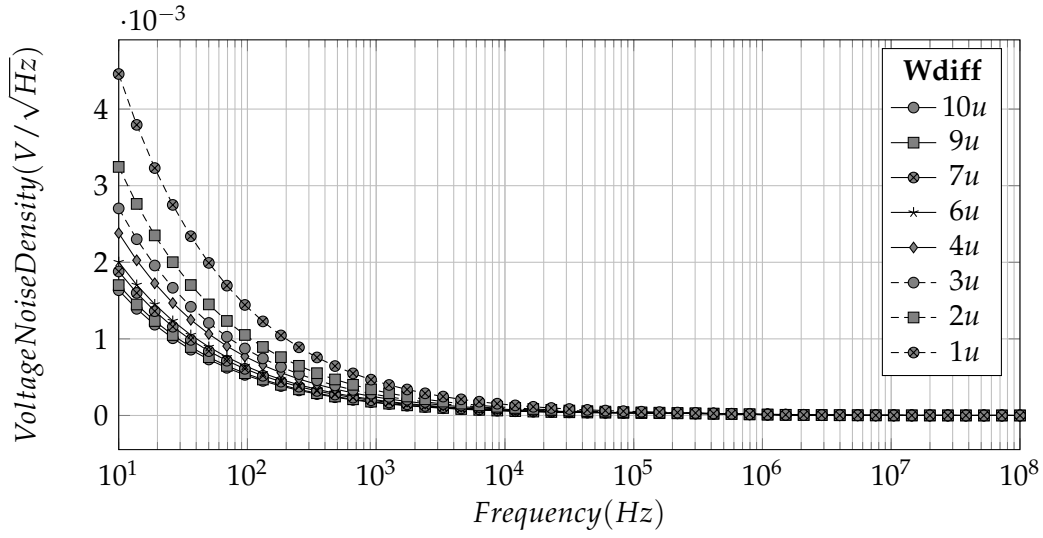


FIGURE 4.5: Voltage Noise Density dependence on the differential pair transistor width.

The gain seems to not be affected in the lower frequencies but at higher ones we can clearly see some slight difference on the maximum frequency bandwidth at higher gain values. When $wdiff = 10um$, the frequency bandwidth is the biggest and thus that value is selected. Moreover, as seen in FIGURE:4.5 when the width of the transistor pair is set at $10um$, the $1/f$ noise profile is also at its lowest.

The differential amplifier also consists of a current mirror which acts as its load. The length once again stays at $130nm$ and the width ($wmirr$) is varied from $1um$ to $10um$ with a step of $1um$ (TOP FIGURE:4.6).

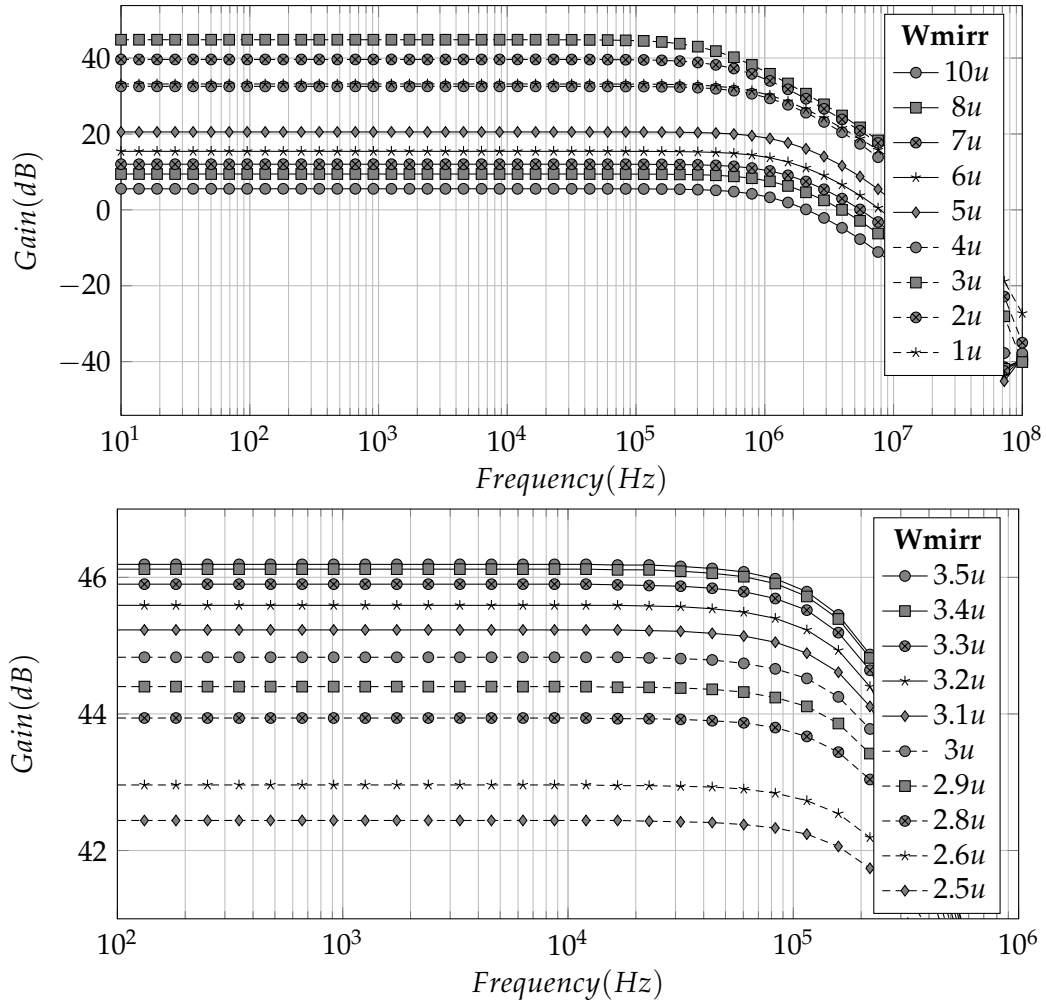


FIGURE 4.6: Gain dependence on the load current mirror transistors width.

Seems like $3um$ is the best value to choose since that gives the highest open-loop gain

but since the deviation between two consecutive values of um is so high, a second analysis was run to vary $wmirr$ from $2.5um$ to $3.5um$ with a step of $100nm$ (BOTTOM FIGURE:4.6). Here it is evident that just by increasing the width by $500nm$, there is a gain increase of more than $1dB$.

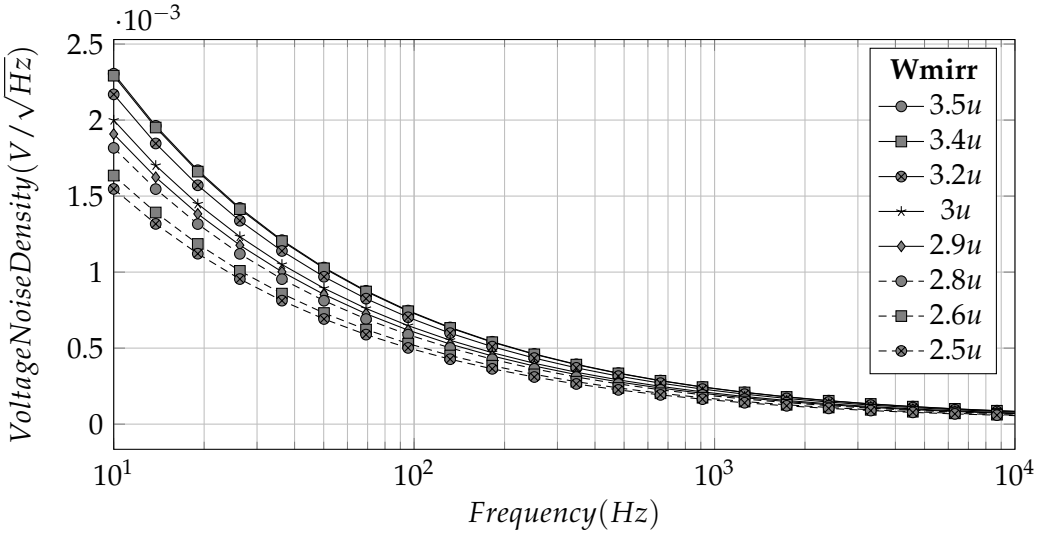


FIGURE 4.7: Voltage Noise Density dependence on the current mirror pair transistor width.

But as seen in FIGURE:4.7, that change in $wmirr$ also has an affect on the noise levels. However, there is no need for gain values higher than $42dB$, the value $2.6um$ is chosen because it provides a great balance between gain and noise.

4.2.2 Common Source Amplifier

As stated in CHAPTER:2, the second stage of the Operational Amplifier is a typical Common Source Amplifier. Once again a parametric analysis is done where the width of the NMOS transistor (wcs) varies between the values $1um$ and $10um$ with a step of $1um$. FIGURE:4.8 shows that for $wcs = 2um$, the gain is about $43dB$.

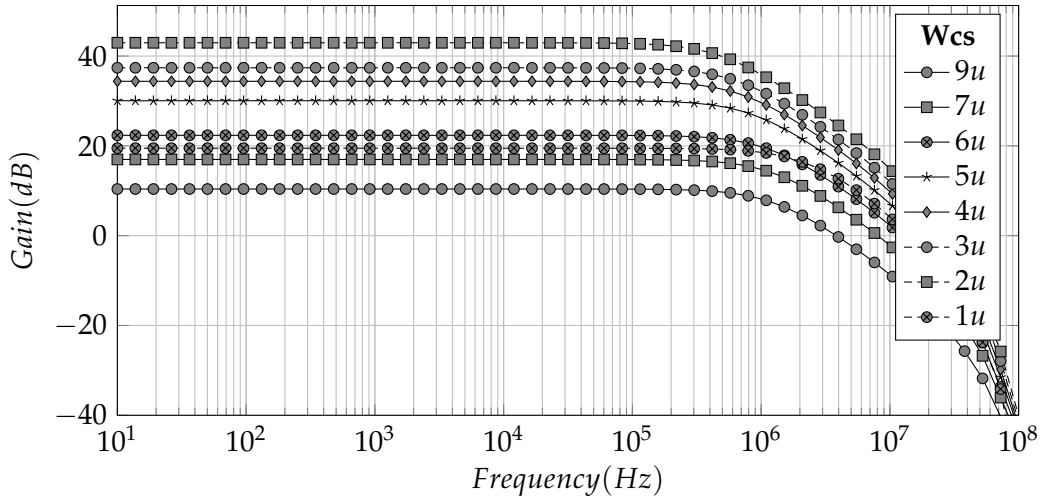


FIGURE 4.8: Gain dependence on the CS transistor width.

But from the noise analysis results as seen in FIGURE:4.9 that particular value also causes the Voltage Noise Density to almost double in magnitude compared to the previous width value of just $1um$.

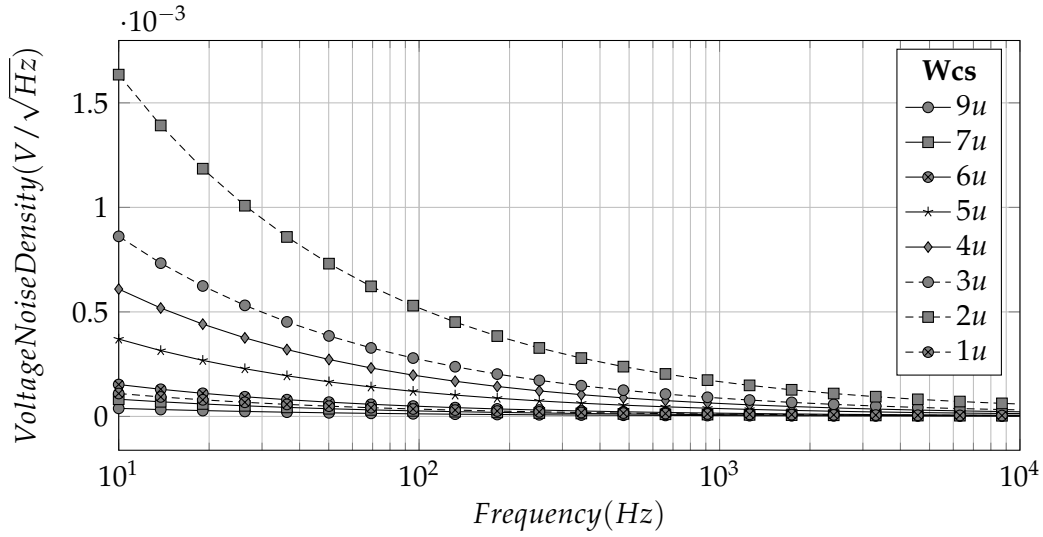


FIGURE 4.9: Voltage Noise Density dependence on the CS transistor width.

To better understand how the width of the Common Source transistor affects the output gain of the Operational Amplifier, a second parametric analysis is done but this time the value of *wcs* changes from $1.5um$ to $2.5um$ with a step of $100nm$. Similarly, one more analysis is executed for the same new width values to view the Voltage Noise Density

values.

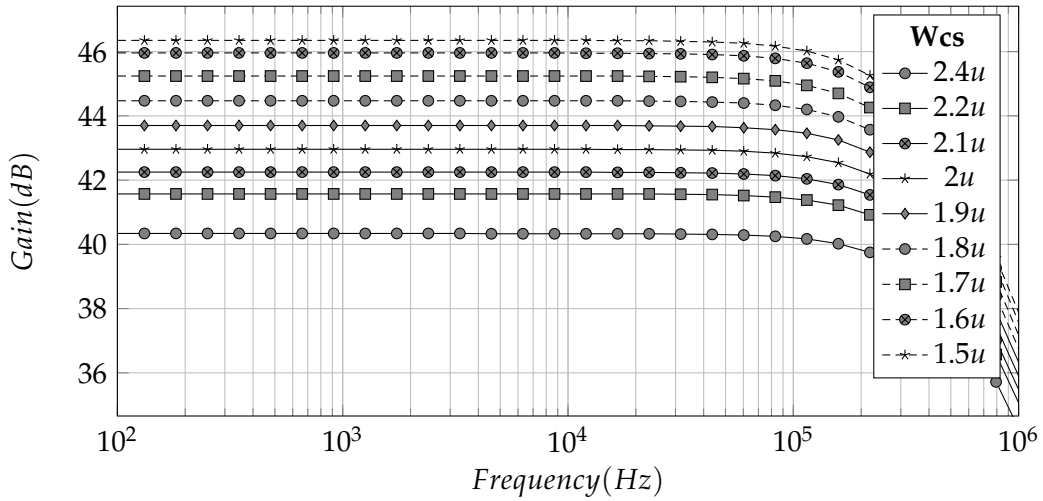


FIGURE 4.10: Gain dependence on the CS transistor width.

In the two FIGURES:4.10 and 4.11 a more in depth look is provided. It seems like there is a value between 1um and 2um that causes the gain to suddenly increase. If there was no consideration about the noise levels the value 1.5um would provide the highest gain. However, noise is a concern in this thesis and thus the width value of 2um was selected instead since it seems to provide a balance between noise and gain.

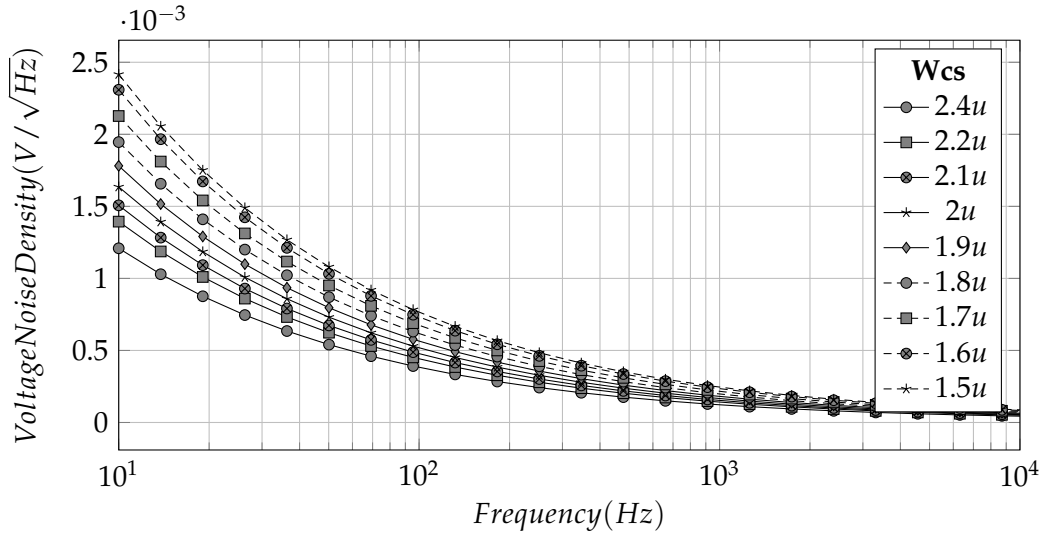


FIGURE 4.11: Voltage Noise Density dependence on the CS transistor width.

In the previous subsection the length of the transistors was kept at $130nm$ but for the Common Source transistor there is a need to slightly alter that value (lcs). As mentioned in SUBSECTION:4.1 the design now features a single supply and the output signal can no longer swing around zero. So a positive DC offset is added to shift the signal upwards. That DC offset depends upon the length of the Common Source transistor and must be fine tuned in order to be at around half the supply voltage ($V_{offset} = VDD/2 = 600mV$). If not, the output signal can get heavily distorted as the amplifier saturates.

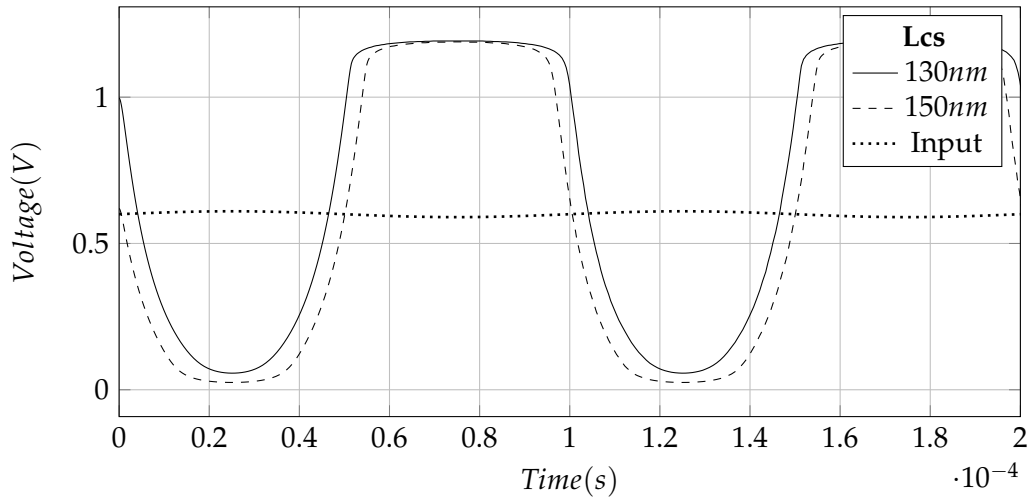


FIGURE 4.12: The output signal swing distortion caused by improper DC offset when in open-loop configuration.

As seen in FIGURE:4.12 the output signal is far from symmetric and is definitely distorted. However, such behaviour, is to be expected because the simulation was done in an open-loop configuration. FIGURE:4.13 shows the output when the Operational Amplifier has a feedback loop. The output signal that corresponds to $130nm$ is centered around $1V$. That leaves a headroom of $1V$ for amplifying the negative half of the signal but only $200mV$ for amplifying the positive one. The result is that the top half gets "chopped off" and the signal is distorted.

Unlike before, the output signal corresponding to the value of $150nm$ is properly centered around half the value of the power supply. This allows both the top and bottom half of the signal to be amplified almost equally. Some distortion at the top of the signal is still visible due to the nature of that type of amplification. For all the reasons above, the value $150nm$ was selected for lcs.

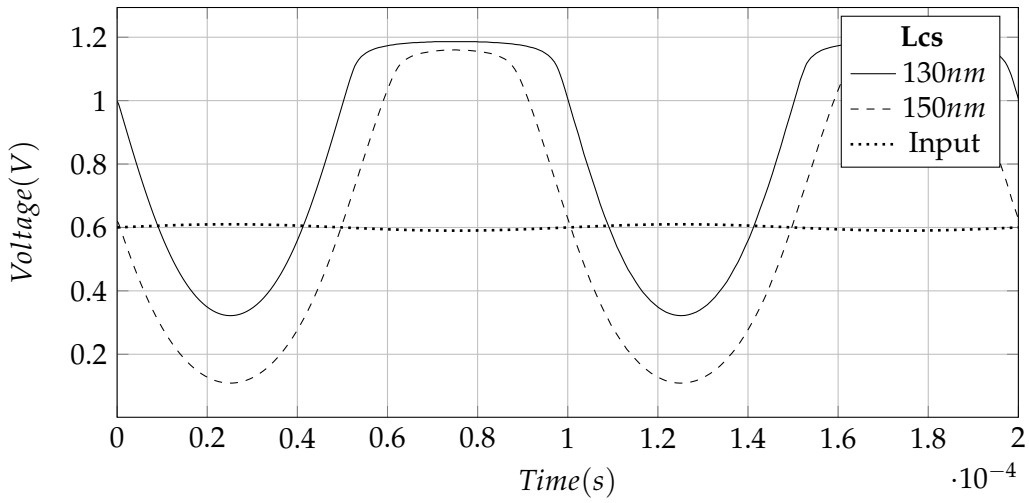


FIGURE 4.13: The output signal swing distortion caused by improper DC offset with a feedback loop.

4.2.3 Power Current Mirror

Simulations did not show any drastic change in the Operational Amplifier's performance when altering the width of the dual output current mirror. The value of 2.5um was selected because it showed a slight increase in the frequency bandwidth.

4.2.4 Miller Capacitor

In SUBSECTION:2.4 the reason for the usage of the Miller Capacitor was explained. Its value is very important for the stability of the Operational Amplifier but it also changes the frequency bandwidth as well. FIGURE:4.14 shows how the frequency bandwidth drastically changes as the Miller capacitor becomes one hundred times larger. The Gain-Bandwidth Product (GBWP) drops from 110MHz down to only 10MHz when the capacitor is set at 100fF.

Having a larger GBWP seems enticing but one must take into consideration other problems that may exist. The biggest problem in closed-loop systems is oscillation. An abrupt change in one of the inputs can cause a chaotic response at the output. This behaviour is unwanted and must be avoided at all costs.

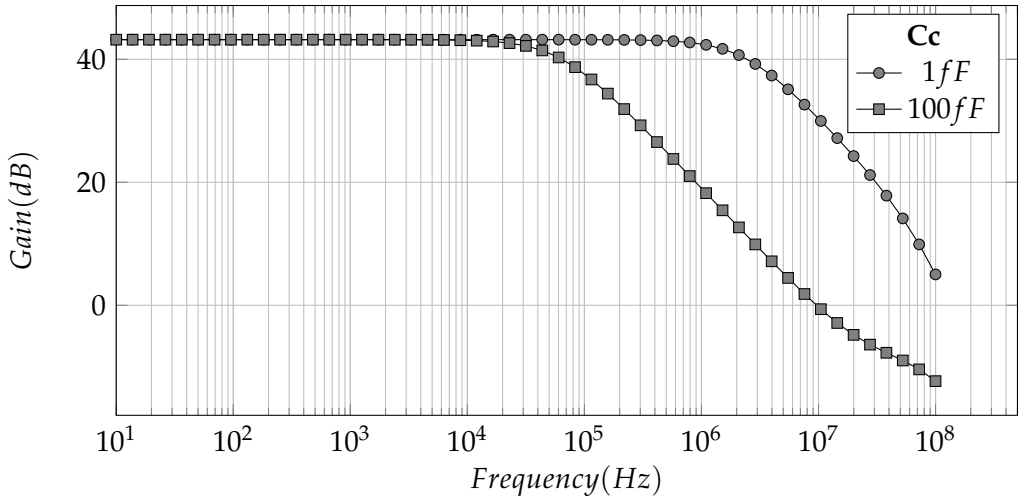


FIGURE 4.14: Op-Amp Bandwidth affected by the Miller capacitor.

To check for such unwanted behaviour, a step response analysis must be done. First, the input circuitry must undergo some modifications. As seen in FIGURE:4.15, the Op-

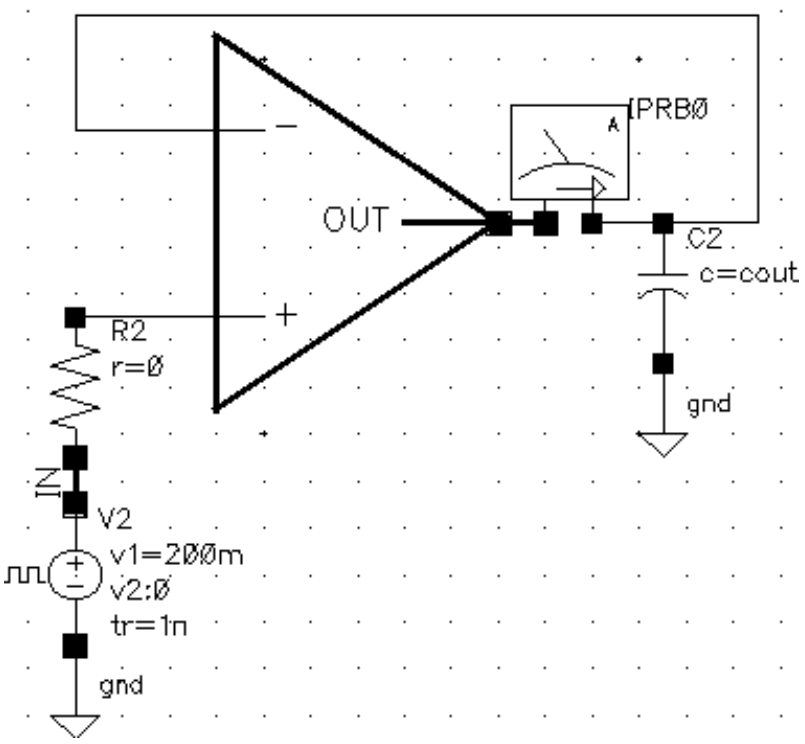


FIGURE 4.15: The testing circuitry for the step response simulation.

erational Amplifier is set up in a non-inverting configuration with a unity gain feedback

loop. The capacitor *cout* is set at $0pF$ for this example and the most important component is the square wave voltage source at the input. This source provides the abrupt change that was mentioned above. The results can be seen in the FIGURE:4.16 and it is clear that a capacitor of $100fF$ and above must be used in order to avoid oscillations.

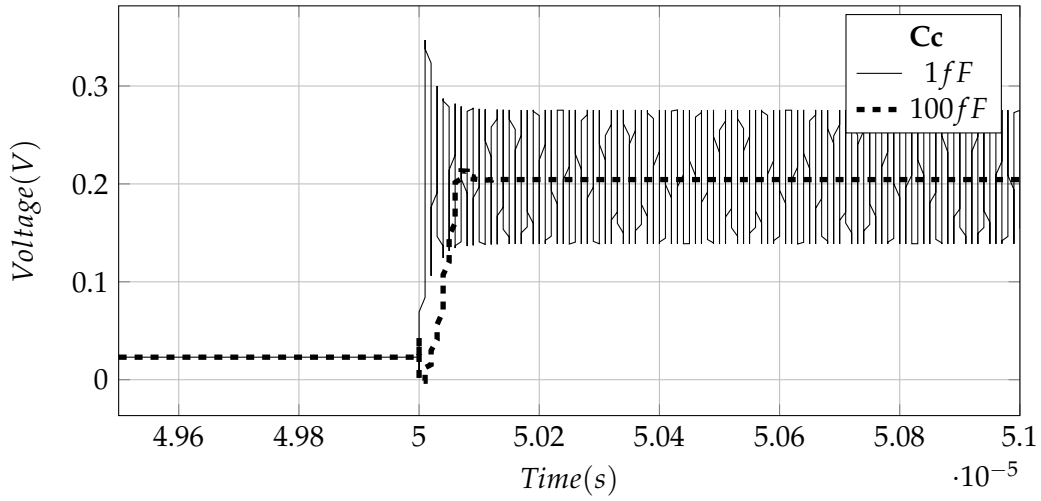


FIGURE 4.16: An improperly selected capacitor value can cause the output to oscillate.

4.2.5 Nullifying Resistor

The nullifying resistor's purpose is to enhance the stability of the Operational Amplifier by shifting the Zeros created by the feed-forward path of the Miller capacitor to the left. It also "spreads" apart the existing Poles thus increasing the stability even more. The addition of a 10Ω nullifying resistor is enough to shift everything to the LHP. FIGURE:4.17 shows the Poles and Zeros before and FIGURE:4.18 shows them after the addition of *rc*.

In FIGURE:4.17 two Zeros exist in the RHP which can add phase lag to the system and erode the phase margin of the design. Moreover, even though it is not clearly visible, the Pole that seems to be at (0,0) is actually in the RHP as well. That indicates a possible state in which the Operational Amplifier may become unstable and oscillate.

Simply by adding the nullifying resistor, most of those problems can be avoided. FIGURE:4.18 shows that all the poles have now been relocated to the LHP and furthermore, they have been split apart, thus increasing the stability. A relocation of the Zeros has also been done but one Zero remains in the RHP though it can be moved further to the left by increasing the value of the Miller capacitor.

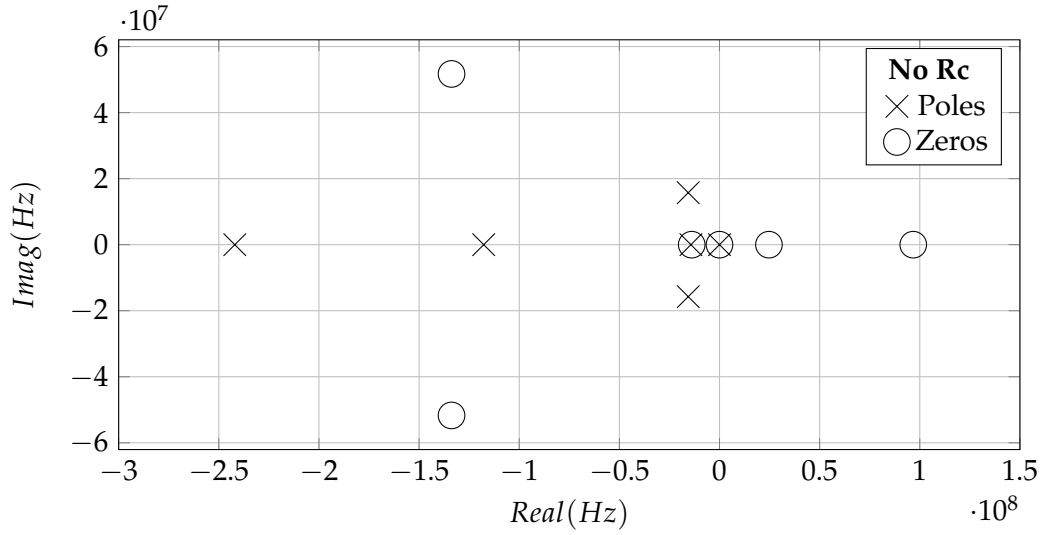


FIGURE 4.17: The Pole-Zero plot with no nullifying resistor.

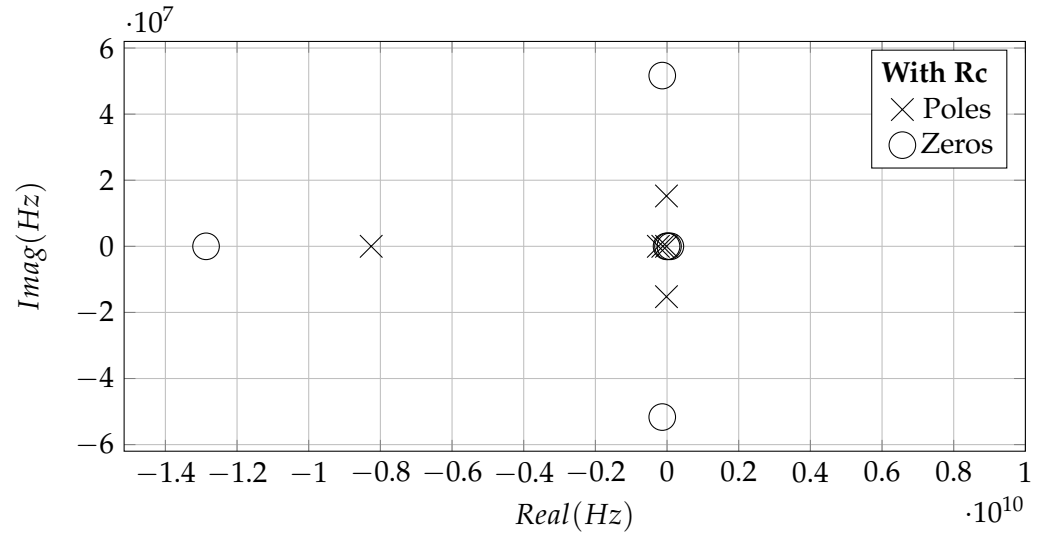


FIGURE 4.18: The Pole-Zero plot with a nullifying resistor.

4.2.6 Gain and Phase Margins

Margin is the extra amount of something that can be used when needed. Here, the idea of Gain and Phase Margins is exactly that. Gain margin indicates how much extra gain the design can output before falling into a potentially unstable state. Similarly, phase margin indicates how much extra phase shift can be added before the system falls once again into an unstable state and starts to oscillate. Calculating those two values of margin

can be done easily by examining the gain and phase Bode plots of a stability analysis. The FIGURE:4.19 shows the two plots.

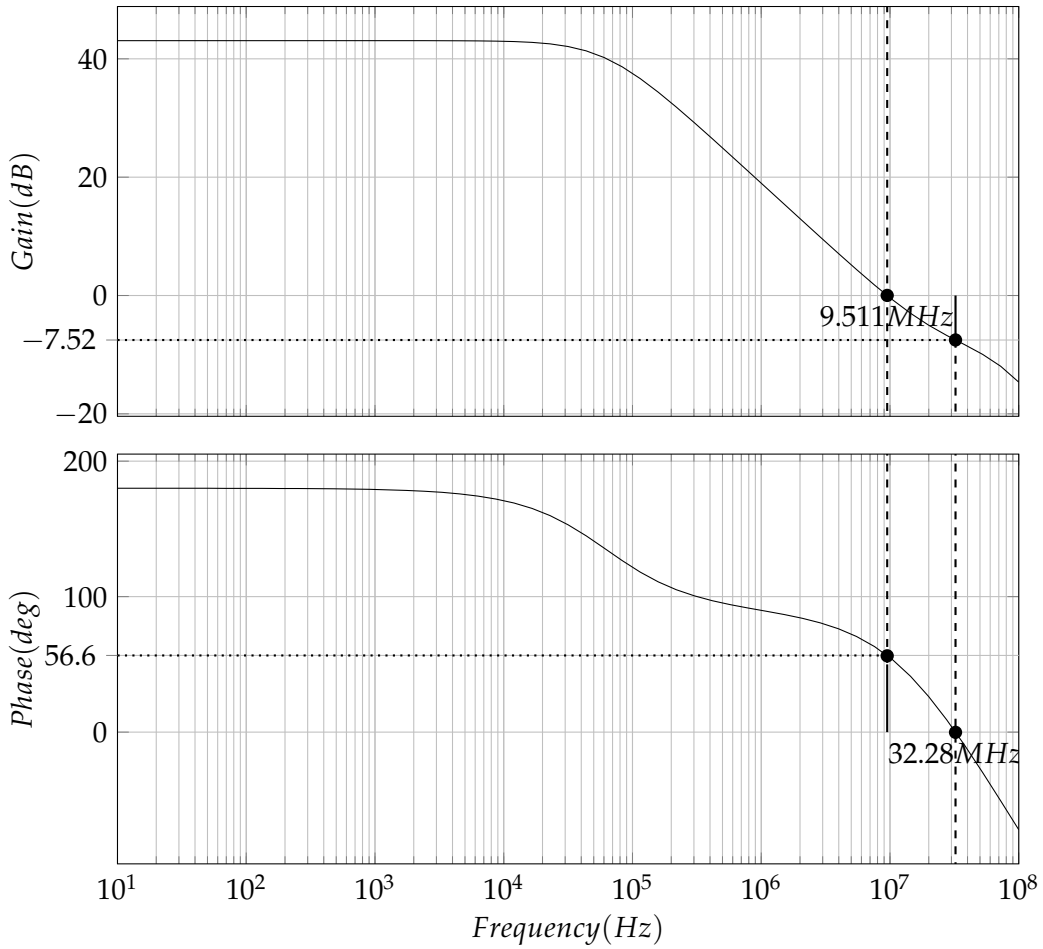


FIGURE 4.19: Extracting Gain and Phase margins from the stability Bode plots.

To calculate the Gain Margin from the Bode plots the point where the phase reaches 0° must be found first. That happens at $32.28MHz$. Now this specific frequency corresponds at a gain value in the gain Bode plot. That value is named Gain Margin and for this design it is $7.52dB$. The Phase Margin can be found in a similar way. The frequency value where the gain plot reaches zero is found ($9.511MHz$) and then the phase is calculated at that frequency. So, the Phase Margin is 56.6°.

The Phase Margin is adequate but the Gain Margin is somewhat on the low side. Even though it is within the initial specifications of the design, it would wise to increase it further.

4.2.7 Slew Rate

The Slew Rate is a metric on how fast the output of the Operational Amplifier can change. It is measured in V/s and the higher the value the sharper the output signal. FIGURE:4.20 shows how fast the voltage at the output rises based on the output load capacitor *cout*.

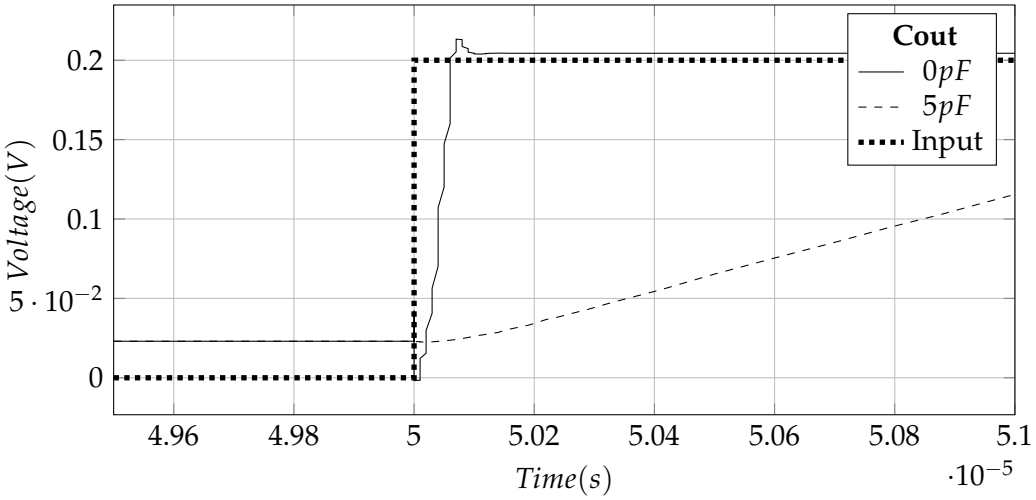


FIGURE 4.20: The slew rate with and without a loaded output.

The slew rate can be calculated by applying the EQUATION:4.1 to a small portion of the signal slope.

$$SR = \frac{\Delta V}{\Delta s} \tag{4.1}$$

For the unloaded output the Slew Rate is about $4.5MV/s$ and with a typical load of $5pF$ it drops down to $102kV/s$. Both of those values are sufficient for this design.

Chapter 5

Conclusion

5.1 Final Design

The final schematic can be seen in FIGURE:5.1 while the component values are presented on TABLE:5.1 along with each transistor's width-length ratio.

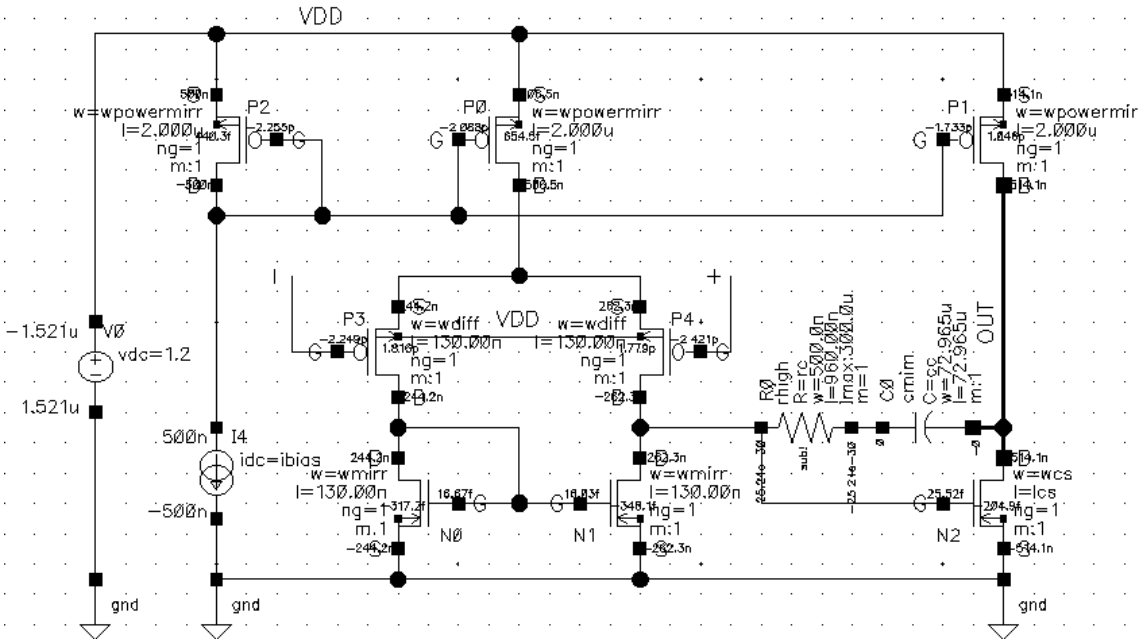


FIGURE 5.1: The final design of the CMOS Operational Amplifier.

So far there has not been a mention of the total DC power consumption of the Operational Amplifier. That is because the power consumption should be measured during the very final stages of the design to get an accurate result. The voltage source in the FIGURE:5.1 shows both the supply voltage and the total DC current flowing through it.

Simply by using the EQUATION:5.1, the DC power consumption can be calculated.

$$P = VI \tag{5.1}$$

For $V = 1.2V$ and $I = 1.52uA$ we get a total power consumption of $1.824uW$. If we were to power the Operational Amplifier from a single watch battery with an average capacity of $200mAh$ it would last for 12.5 years!

Component Parameter	**Value**
ibias	$500nA$
wpowermirr	$2.5um$
wdiff	$10um$
wmirr	$2.6um$
wcs	$2um$
lcs	$150nm$
cc	$100fF$
rc	10Ω

Transistor	**(W/L) Ratio**
P0	1.25
P1	1.25
P2	1.25
P3	76.9
P4	76.9
N0	20
N1	20
N2	13.3

TABLE 5.1: The final values selected for the component parameters and transistor sizes.

The final results of the frequency response of the Operational Amplifier can be seen in the FIGURE:5.2. The maximum open-loop gain is $43dB$ and the GBWP is $9.72MHz$.

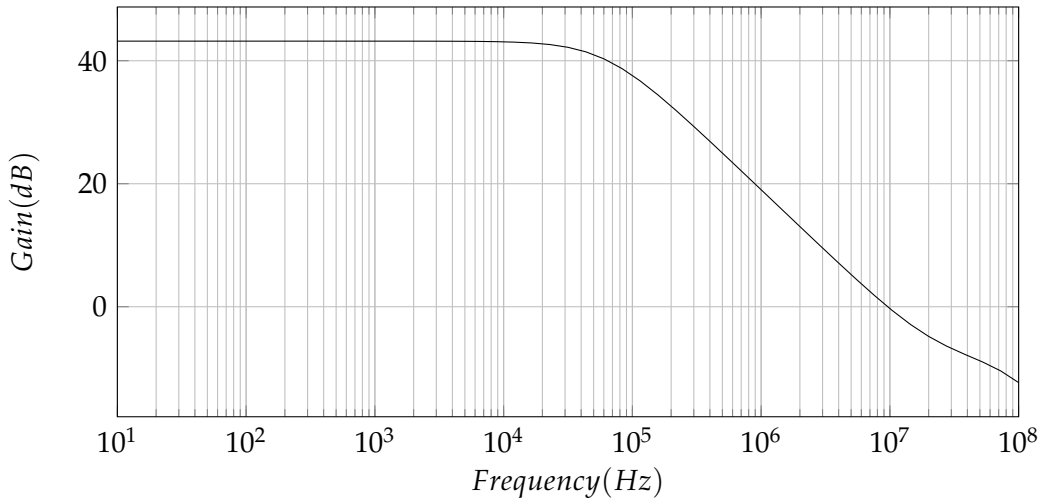


FIGURE 5.2: The final open-loop gain plot.

Similarly for the noise output, FIGURE:5.3 shows the equivalent input noise and which was measured with the Operational Amplifier being in a unity gain configuration. The absolute maximum is $11.2uV$ @ $10Hz$ and the noise corner frequency is about $100Hz$. At a frequency of $1kHz$ the noise drops to a value of $1.14uV$.

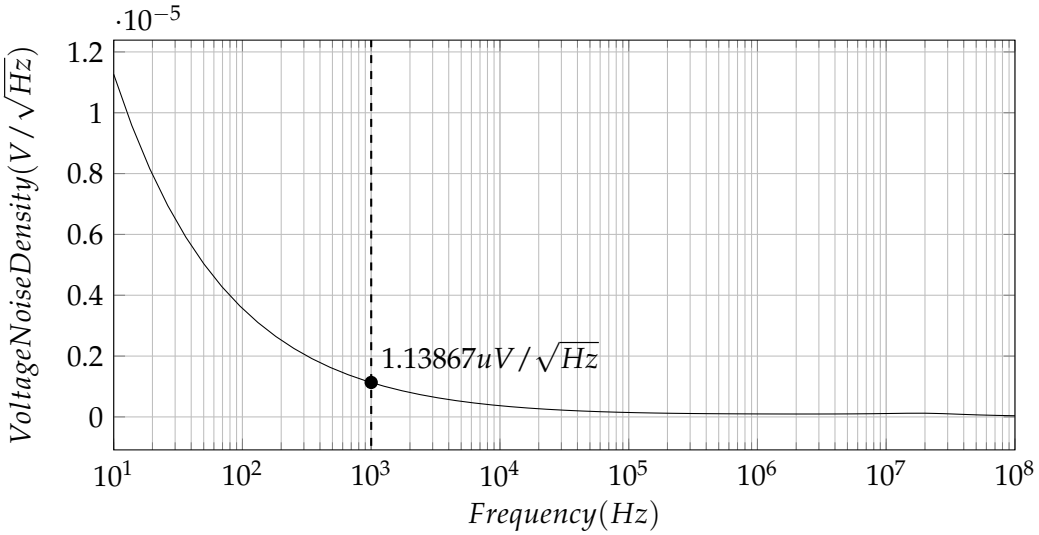


FIGURE 5.3: Voltage Noise Density plot at a unity gain configuration.

TABLE:5.2 shows all the final specifications that were the result of many hours of studying, designing and simulations. All of them satisfy the original criteria that were first presented in the introduction of this thesis.

Parameter	**Value**
DC Supply	$1.2V$
Open-loop Gain	$43dB$
Gain-Bandwidth Product	$9.72MHz$
Power Consumption	$1.824uW$
Voltage Noise Density ($f = 1kHz$)	$1.13867uV/\sqrt{Hz}$
Gain Margin	$7.521dB$
Phase Margin	56.6°
Slew Rate (No Load)	$4.55MV/s$
Slew Rate ($5pF$ Load)	$102kV/s$

TABLE 5.2: A table with all the final specifications of the Operational Amplifier.

There was a great amount of knowledge gained throughout the whole completion

time of this thesis. Learning how such an important device works is one thing but learning how to design one based on a specific set of characteristics given is a whole different story. One must understand the critical role of every single parameter in order to successfully create such a component, come head to head with the physics of materials and work around unsolvable problems.

5.2 Possible Future Work

By no means is this a perfect design. It has the potential to be improved. For starters, the frequency bandwidth can be expanded to reach the $100MHz$ point. A greater frequency bandwidth can make the Operational Amplifier more versatile by being used in more high frequency applications.

Secondly, the stability of the amplifier, even though it is adequate, has the ability to be further improved. Increasing not only the gain margin but the phase margin as well is probably the best strategy to use to overcome potentially unstable states.

Moreover, some more extensive tests can also be done to include other metrics that have been omitted in this thesis such as the Common Mode Rejection Ratio (CMRR) and the Power Supply Rejection Ratio (PSRR).

And finally, this whole design can go to the layout stage where each and every component is laid out and carefully placed based on placement algorithms and other specifications. This task is big enough to probably seed another extensive thesis.

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