Design Flow, modeling and characterization of Through Silicon Via(TSV), for 3D Integrated circuits

DIPLOMA THESIS

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“Be great in act, as you have been in thought.”

Shakespeare, William

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Contents

List of Figures

List of Tables

Chapter 1. Introduction

English

The main aim of this thesis is to validate and refine ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE's (EPFL's) 3D integration technology, as well as, integrate it to the existing 2D digital design flow in a very transparent, to the designer, manner.

Throughout the years, typical microprocessors and related integrated circuits are aiming towards lower power consumption, increased performance, reduced form factor and increased integration. 3D technology is one of the state of the art, emerging technologies that can provide improvements throughout all the aforementioned areas. For conventional process scaling, the signal delay time is expected to increase with technology node mostly from the increasing resistance of the wires. The situation is more exaggerated because of the constant increase of the interconnect length as well as the increase of the number of interconnect layers used. Thus, mainly for microprocessor systems, it is most important to focus primarily on using 3D to reduce wiring since, in latest analysis, more than 30% of the power in a microprocessor can be considered to be consumed by interconnect. By utilizing 3D integration, multiple layers can be stacked aiming high bandwidth, low latency and low power. Additionally, via the use of 3D integration new microarchitecture opportunities arise that could allow performance, power and area tradeoffs. A main design consideration in 3D microprocessors is to determine the number and type of layers to be integrated. Typical benchmarking analysis can demonstrate the relative benefits of an increased number of layers. Even though a constantly increasing number of layers can result in increased performance, it is clear that the largest benefit occurs from stacking just the first two layers. In addition to the foretold diminishing returns observed while increasing the number of layers, there are also processing issues that may practically limit the number of layers, as well as, complexity in the design process. This thesis aims to reduce the foretold complexity and speed up the whole process.

The thesis commences with an introduction to the 3D integration technology. In the next chapter the most critical component, namely Through Silicon Via (TSV), is modeled physically and five different TSV models are discussed. More specifically, the TSV is a vertical interconnection method between chips and also is the critical enabling technology for three-dimensional integrated circuits (3D ICs). TSV resistance, inductance, and capacitance need to be modeled to determine their impact on the performance of a 3-D circuit.

The thesis then proceeds with a chapter dedicated to Radiofrequency TSV measurements been performed aiming to model TSVs accurately. More particularly, the TSVs consist of parasitics and also from a MOS-capacitor whose value is critical to measure since it can affect significantly the overall emulation of the behavior of a TSV. Many mathematical models have attempted to calculate this value. The RF measurement procedure and also the equipment used are described. The measurement results will be presented in the form of histograms. Additionally, the aim of this chapter is on the one hand to validate the value of MOS-capacitor extracted by theoretical mathematic models with the experimental measurements and from the other hand to find the proper value for MOS-capacitor to demonstrate their behavior. Extracting the correct value of MOS-capacitor can be the beginning for TSV model expansion in the future.

The thesis then proceeds with a chapter dedicated to a number of Computer Aided Design (CAD) tools developed throughout the course of this thesis aiming to automate and speedup a lot of

critical and time intensive parts of the 3D integration flow. The CAD tools developed aim to extend the current standard digital design flow of 2D into a 3D flow with the minimum involvement of the designer.

The next chapter describes the procedure of physical layout of a TSV transmitter and receiver to be used in par with the TSV models developed earlier. In the previous chapters we mentioned the first steps, create a TSV model, analyze timing parameters, convert .cir files to .lib files and use them in the Synopsys Design Compiler to conclude with the final step, the final circuit creation. Specifically, this chapter concentrates on creating a final product and it describes step by step this process. The schematic of the TSV model chosen to be create and the final physical layout from the schematic is also discussed. The thesis then concludes with a chapter devoted to conclusions and future work.

Ελληνικά

Ο κύριος σκοπός της διπλωματικής αυτής εργασίας είναι να επικυρώσει και να βελτιώσει την τρισδιάστατη τεχνολογία ολοκλήρωσης του ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE (EPFL), καθώς και να την ενσωματώσει στην υπάρχουσα δισδιάστατη ψηφιακή ροή σχεδιασμού μια ιδιαίτερα διαφανή, για τον σχεδιαστή, διαδικασία.

Όλα αυτά τα χρόνια, οι τυπικοί μικροεπεξεργαστές καθώς και τα σχετικά ολοκληρωμένα κυκλώματα στοχεύουν προς την χαμηλότερη κατανάλωση ενέργειας, την αύξηση της απόδοσης,τη μειωμένη μορφή παράγοντα και την αυξανόμενη κλίμακα ολοκλήρωσης. Η τρισδιάστατη τεχνολογία ολοκλήρωσης είναι ένας από τους πλέον εξελισσόμενους τομείς της τεχνολογίας, τομείς που μπορούν να παρέχουν βελτιώσεις σε όλες τις ανωτέρω περιοχές. Κατά την συμβατική κλιμάκωση της τεχνολογίας, ο χρόνος καθυστέρησης του σήματος αναμένεται να αυξηθεί με τον κόμβο της τεχνολογίας, ως επί το πλείστον από την αυξανόμενη αντίσταση των καλωδίων. Η κατάσταση καθίσταται πιο κρίσιμη λόγω της συνεχούς αύξησης του μήκους διασύνδεσης καθώς και την αύξηση του αριθμού των στρωμάτων που χρησιμοποιούνται για την διασύνδεση. Ετσι, κυρίως για τα συστήματα μικροεπεξεργαστών, είναι πιο σημαντικό να εστιάζονται πρωτίστως στην χρήση τριών διαστάσεων ώστε να μειώθει το μήκος της διασύνδεσης, διότι, σύμφωνα με πρόσφατες αναλύσεις, περισσότερο από το 30% της ισχύος σε έναν μικροεπεξεργαστή μπορεί να θεωρηθεί ότι καταναλώνεται στην διασύνδεση. Με τη χρήση τρισδιάστατης ολοκλήρωσης, πολλαπλά στρώματα μπορούν να στοιβάζονται στοχεύοντας σε υψηλό εύρος ζώνης, χαμηλή καθυστέρηση και χαμηλή ισχύ. Επιπλέον, μέσω της χρήσης της τρισδιάστατης ολοκλήρωσης νέες ευκαιρίες προκύπτουν σε επίπεδο μικροαρχιτεκτονικής που θα μπορούσαν να προσφέρουν βελτιώσεις στην απόδοση, την απαιτούμενη ισχύ και την επιφάνεια ολοκληρωμένου. Ένα κύριο μέλημα της τρισδιάστατης ολοκλήρωσης για τους μικροεπεξεργαστές είναι να προσδιοριστεί ο αριθμός και το είδος των επιπέδων που πρόκειται να ενσωματωθούν. Τυπική ανάλυση μέσω συγκριτικής αξιολόγησης μπορεί να αποδείξει τα σχετικά οφέλη από την αύξηση του αριθμού των επιπέδων. Ακόμη και αν ένας συνεχώς αυξανόμενος αριθμός επιπέδων μπορεί να οδηγήσει σε αυξημένη απόδοση, είναι σαφές ότι το μεγαλύτερο όφελος προκύπτει από το στοίβαγμα μόνο των πρώτων δύο επιπέδων. Εκτός από τις προαναφερθείσες μειώσεις στα οφέλη κατά την αύξηση του αριθμού των επιπέδων, υπάρχουν επίσης προβλήματα επεξεργασίας που μπορούν να περιορίσουν ουσιαστικά τον αριθμό

των στρώσεων, καθώς και πολυπλοκότητα κατά την διαδικασία σχεδιασμού. Η εργασία αυτή έχει ως στόχο να μειώσει την πολυπλοκότητα και να επιταχύνει την όλη διαδικασία.

Η διατριβή ξεκινά με μια εισαγωγή στην τεχνολογία τρισδιάστατης ολοκλήρωσης. Στο επόμενο κεφάλαιο το πιο κρίσιμο συστατικό, ονόματι του Through Silicon Via (TSV), μοντελοποιείται σε φυσικό επίπεδο και επιπλέον πέντε διαφορετικά μοντέλα TSV συζητούνται. Ειδικότερα, η τεχνολογία των TSV είναι μία κατακόρυφη μέθοδος διασύνδεσης μεταξύ των τσιπ και επίσης είναι η απαραίτητη τεχνολογία που επιτρέπει τα τρισδιάστατα ολοκληρωμένα κυκλώματα (3D ICs). Η αντίσταση, αυτεπαγωγή, χωρητικότητα των TSV πρέπει να μοντελοποιηθεί για να καθοριστεί ο αντίκτυπός τους στην απόδοση του τρισδιάστατου κύκλωματος.

Η διατριβή προχωρά στη συνέχεια με ένα κεφάλαιο αφιερωμένο σε μετρήσεις ραδιοσυχνοτήτων των TSV που έχουν πραγματοποιηθεί με στόχο να δημιουργηθούν μοντέλα TSVs με ακρίβεια. Πιο συγκεκριμένα, τα TSVs αποτελούνται από παρασιτικά και επίσης από ένα πυκνωτή MOS-των οποίων η τιμή είναι κρίσιμο να μετρηθεί καθώς μπορεί να επηρεάσει σημαντικά τη συνολική προσομοίωση της συμπεριφοράς ενός TSV. Πολλά μαθηματικά μοντέλα έχουν προσπαθήσει να υπολογίσουν αυτές τις τιμές. Η διαδικασία μέτρησης ραδιοσυχνοτήτων και επίσης ο χρησιμοποιούμενος εξοπλισμός περιγράφεται. Τα αποτελέσματα των μετρήσεων παρουσιάζονται με τη μορφή ιστογραμμάτων. Επιπλέον, ο στόχος του κεφαλαίου αυτού είναι αφενός να επικυρώσει την τιμή του μεγέθους του πυκνωτή MOS- προερχόμενη από το θεωρητικό υπολογισμό μαθηματικών μοντέλων με τις πειραματικές μετρήσεις και από την άλλη πλευρά να βρει την κατάλληλη τιμή για MOS-πυκνωτή για να επιδείξει τη συμπεριφορά τους. Η εξαγωγή της σωστής τιμής του πυκνωτή MOS-μπορεί να είναι η αρχή για την επέκταση των μοντέλων TSV στο μέλλον.

Στη συνέχεια η διατριβή προχωρά με ένα κεφάλαιο αφιερωμένο σε μια σειρά από Computer Aided Design (CAD) εργαλείων που έχουν αναπτυχθεί σε όλη τη διάρκεια αυτής της εργασίας με στόχο την αυτοματοποίηση και επιτάχυνση των πλέων κρίσιμων και χρονοβόρων τμήματων της τεχνολογίας τρισδιάστατης ολοκλήρωσης. Τα εργαλεία CAD αναπτύχθηκαν με τρόπο τέτοιο ώστε να αποτελούν επέκταση στο σημερινό πρότυπο ψηφιακής ροής του δισδιάστατου σχεδιασμού σε ροή τριών διαστάσεων με την ελάχιστη συμμετοχή του σχεδιαστή.

Το επόμενο κεφάλαιο περιγράφει τη διαδικασία της φυσικής διάταξης του πομπού και του δέκτη TSV ώστε να χρησιμοποιηθεί στο ίδιο επίπεδο με τα μοντέλα TSV που αναπτύχθηκαν νωρίτερα. Στα προηγούμενα κεφάλαια αναφερθήκαμε στα πρώτα βήματα, δημιουργία ενός μοντέλου TSV, ανάλυση των παραμέτρων χρονισμού, τη μετατροπή .CIR αρχείων σε .Lib αρχεία και η χρήση τους στον Design Compiler τις Synopsys ώστε να καταλήξουμε στο τελικό βήμα, την δημιουργία του τελικού κύκλωματος. Ειδικότερα το κεφάλαιο αυτό επικεντρώνεται στη δημιουργία ενός τελικού προϊόντος και περιγράφει βήμα προς βήμα τη διαδικασία. Η σχηματική απεικόνιση του μοντέλου TSV που επιλέχθηκε να χρησιμοποιηθεί και η τελική φυσική διάταξη από το σχηματικό συζητείται επίσης. Η εργασία ολοκληρώνεται έπειτα με ένα κεφάλαιο αφιερωμένο στα συμπεράσματα και τις μελλοντικές εργασίες.

Français

L'objectif principal de cette Thèse est de valider et d'affiner la technologie d'intégration 3D au l'Ecole Polytechnique Fédérale de Lausanne (EPFL), ainsi que, de l'intégrer au flux existant de conception 2D numérique dans un très transparent, pour le concepteur, manière.

Au fil des ans, les microprocesseurs et les caractéristiques liées à circuits intégrés visent à faible consommation d'énergie, des performances accrues, facteur de forme réduit et une plus grande intégration. La technologie 3D est l'une des règles de l'art, les technologies émergentes qui peuvent fournir des améliorations dans tous les domaines précités. Pour l'extension procédé classique, le temps de retard du signal devrait augmenter avec nœud technologique principalement de l'augmentation de la résistance des fils. La situation est plus accentuée en raison de l'augmentation constante de la longueur d'interconnexion ainsi que l'augmentation du nombre de couches d'interconnexion utilisés. Ainsi, principalement pour des systèmes à microprocesseurs, il est plus important de se concentrer principalement sur l'utilisation de 3D pour réduire le câblage puisque, en dernière analyse, plus de 30% de la puissance dans un microprocesseur peut être considérée comme étant consommée par interconnexion. En utilisant l'intégration 3D, plusieurs couches peuvent être empilées visant une large bande passante et à faible latence et à faible puissance. En outre, grâce à l'utilisation de l'intégration 3D de microarchitecture opportunités surgissent de nouvelles qui pourrait permettre à des compromis de performance, de puissance et de la zone. Un examen de conception principale dans les microprocesseurs 3D est de déterminer le nombre et le type de couches à intégrer. Analyse comparative typique peut démontrer les avantages relatifs d'une augmentation du nombre de couches. Même si un nombre sans cesse croissant de couches peut se traduire par des performances accrues, il est clair que le plus grand avantage de l'empilement se produit seulement les deux premières couches. En plus des rendements décroissants prédits observées tout en augmentant le nombre de couches, il ya aussi des problèmes de traitement qui peut pratiquement limiter le nombre de couches, ainsi que, de la complexité du processus de conception. Cette thèse vise à réduire la complexité annoncée et d'accélérer l'ensemble du processus.

La Thèse commence par une introduction à la technologie d'intégration 3D. Dans le chapitre suivant, le composant le plus critique, à savoir Through Silicon Via (TSV), est modélisé physiquement et cinq différents modèles TSV sont discutées. Plus précisément, le TSV est un procédé d'interconnexion verticale entre les puces et est également la technologie habilitante en trois dimensions (3D circuits intégrés CI). TSV résistance, l'inductance et capacitance doivent être modélisées afin de déterminer leur impact sur les performances d'un circuit en 3-D.

La Thèse procède alors à un chapitre consacré aux mesures de radiofréquences TSV été effectuées en vue de modéliser avec précision TSV. Plus particulièrement, le TSV se composent de parasites et aussi d'un condensateur MOS dont la valeur est essentielle à mesurer car il peut affecter de manière significative l'émulation globale du comportement d'un TSV. De nombreux modèles mathématiques ont tenté de calculer cette valeur. La procédure de mesure RF et également le matériel utilisé sont décrits. Les résultats de mesure sont présentés sous forme d'histogrammes. En outre, l'objectif de ce chapitre est d'une part de valider la valeur du condensateur MOS extraites par les modèles théoriques mathématiques avec les mesures expérimentales et de l'autre main pour trouver la

bonne valeur pour condensateur MOS de démontrer leur comportement. Extraire la valeur correcte de condensateur MOS peut être le début de l'expansion du modèle TSV à l'avenir.

La Thèse procède alors à un chapitre consacré à un certain nombre de Conception Assistée par Ordinateur (CAO) développés tout au long de cette thèse vise à automatiser et accélérer un grand nombre de critiques et de temps parties intensives de l'intégration 3D de flux. Les outils de CAO développé pour objectif d'étendre le flux de courant standard de conception numérique de 2D en 3D avec un débit minimum de la participation du concepteur.

Le chapitre suivant décrit la procédure de configuration physique d'un émetteur et d'un récepteur TSV pour être utilisé dans la hauteur des modèles développés précédemment TSV. Dans les chapitres précédents, nous avons mentionné les premières étapes, de créer un modèle TSV, d'analyser les paramètres de synchronisation, de convertir les fichiers. CIR. Lib et les utiliser dans le Synopsys Design Compiler de conclure avec la dernière étape, la création circuit final. Plus précisément, ce chapitre se concentre sur la création d'un produit final et il décrit étape par étape de ce processus. Le schéma du modèle TSV choisi d'être créer et la mise en page finale du schéma physique est également discutée. La Thèse conclut alors avec un chapitre consacré aux conclusions et travaux à venir.

Chapter 2. TSV models and timing analysis for different coupling scenarios

In this chapter physical modeling of TSV's and five different TSV models we investigated will be discussed thoroughly. More specifically, the TSV is a vertical interconnection method between chips and also is the critical enabling technology for three-dimensional integrated circuits (3D ICs).TSV resistance, inductance, and capacitance need to be modeled to determine their impact on the performance of a 3-D circuit.

After a small introduction on TSV the RLC parameters of the TSV as function of physical parameters and material characteristics are described. Finally, this chapter also proposes some TSV models that can be used to simulate 3-D integrated. A very useful point in this chapter is the signal delay and the different potential at the edges of the TSV's capacitor as a result of timing analysis.

2.1 About TSV

In electronic engineering, a through-silicon via (TSV) is a vertical electrical connection passing completely through a silicon wafer or die. TSVs are a high performance technique used to create 3D integrated circuits, compared to alternatives such as package-on-package, because the density of the vias (Vertical Interconnect Accesses) is substantially higher, and because the length of the connections is shorter. A 3D integrated circuit (3D IC) is a single integrated circuit built by stacking silicon wafers and/or dies and interconnecting them vertically so that they behave as a single device. By using TSV technology, 3D ICs can pack a great deal of functionality into a small “footprint.” The different dice in the stack may be heterogeneous, e.g. combining CMOS logic, DRAM and III-V materials into a single IC. In addition, critical electrical paths through the device can be drastically shortened, leading to faster operation.

The structural complexity of 3D, is treated as equivalent cylindrical structure. 3-D usually includes a conical cylindrical TSV both the top and bottom metal landing.

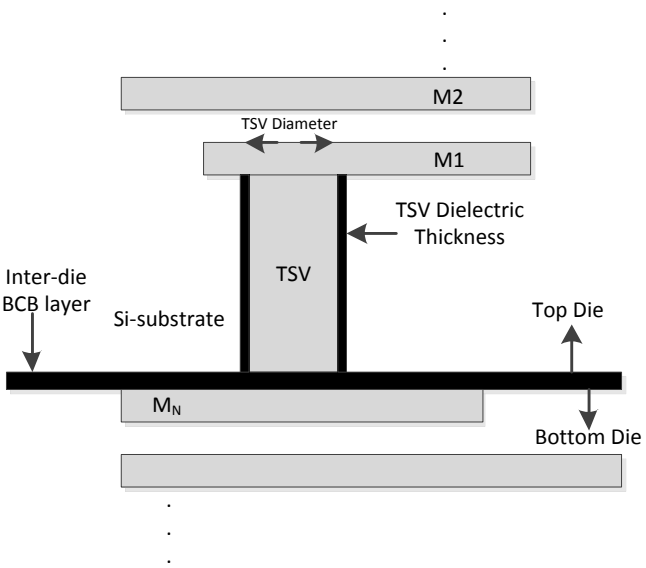


Figure 2-1 Cross section of a TSV

TSV offers several attractive advantages. TSV allows for shorter interconnects between the die, reducing power consumption caused by long horizontal wiring, and eliminating the space and power wasted by buffers (repeaters that propel a signal through a lengthy circuit). TSV also reduces electrical parasitics in the circuit (i.e., unintended electrical effects), increasing device switching speeds. Moreover, TSV accommodates much higher input/output density than wire bonding, which consumes much more space.

The through silicon via is a key component for interconnecting chips vertically and forms a cylindrical metal oxide semiconductor capacitor. In this case the TSV metal acting as a gate and the substrate of the conductor acting as a bulk.

Why a 3D integrated circuit?

In contrast to conventional circuits 2D, 3D integrated circuits offer a new model that builds multiple layers of active devices stacked over each other. Recent developments in process technology have brought 3D technology to the point where it is feasible and practical, and has raised intense interest in the chip industry. The move to 3D allows many benefits over 2D, such as reduced interconnect lengths, improved calculation per unit volume, and the possibility of integrating heterogeneous systems. However, the example requires a significant change from the modern design methodologies, as an optimal 3D chip design has very different characteristics from the optimal design of the chip 2D.

Traditional scaling of semiconductor chips, also improves the speed of propagation of the signal. However, scaling from current manufacturing technologies and chip design has become more difficult, partly because the power density limitations, and partly because linking not done more quickly, while making transistors 3-D integrated circuits were proposed invented to address the challenge of scaling by stacking 2-D dies and connecting them in the 3-d dimension. This promises to speed up communication between the chip layers, 3D ICs promise significant benefits, including:

Footprint

More functionality fits into a small space. This extends Moore's Law and allows a new generation of tiny but powerful devices

Cost

Partitioning a large chip into multiple smaller dies with 3D stacking can improve performance and reduce manufacturing costs, if an individual dies are tested separately.

Heterogeneous integration

Circuit layers can be built with different processes or even different types of wafers. This means that components can be optimized much more than if they had built together in a single wafer. Moreover, data incompatibility with the construction could be combined into a single 3D IC.

Shorter interconnect

The average wire length is reduced. Common data reported by researchers in the order of 10-15%, but this is particularly true for greater connectivity, which can affect delay circuit with a larger amount. Since the 3D cables have much higher capacity than conventional cable-die delay circuit may or may not be improved.

Power

Holding an on-chip signal can reduce energy consumption by 10-100 times. Most cables also reduce energy consumption by producing less parasitic capacitance. The reduction in budget authority resulting in less heat, prolonged battery life and lower operating costs.

Design

The vertical dimension adds a higher class of the connection and opens up new design possibilities.

Circuit security

The stack structure complicates efforts to reverse engineer the circuit. Sensitive circuits can also be divided between the layers in such a way as to obscure the function of each layer.

Bandwidth

3D integration allows for a large number of vertical vias between layers. This allows the construction of bandwidth buses between functional blocks at different levels. A typical example would be a processor + 3D stack memory with the cache stacked on top of the processor. This arrangement allows a much wider bus than the typical 128 or 256 bits between the processor and memory cache.

2.2 *R*TSV, *L*TSV, AND *C*TSV Modeling

In this section we will analyze the basic circuit elements that the TSV consist of. In the picture below we can see a single TSV with its parasitic.

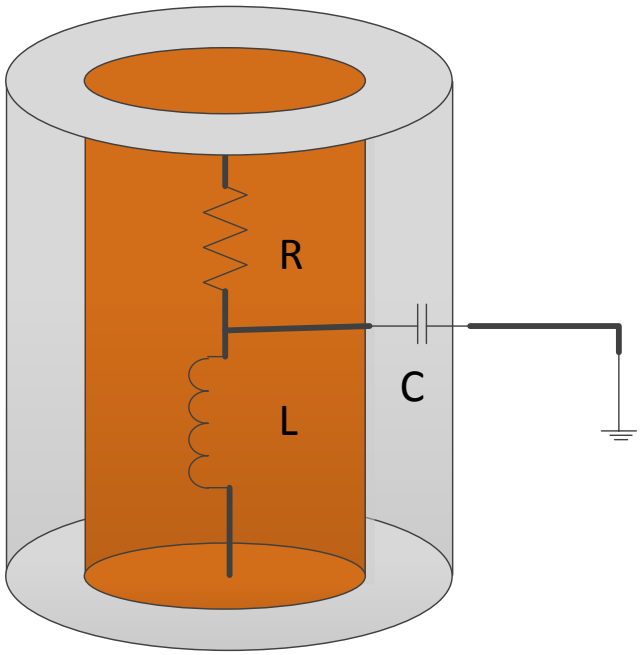


Figure 2-2 Model of a single TSV

- RTSV Model

The analytical expression of the dc resistance of the TSV is given by

$R_{TSV\_DC} = \frac{\rho lTSV}{\pi r2}$

Where ρ is the resistivity of the metal, r the metal radius and l_{TSV} represent the length of the TSV.

For high frequency signals, however, the increase in resistance due to the influence of the skin should be accounted. Specifically, the skin effect increases the effective resistance of the metal with frequency. The equation for skin effect is given by :

$Rac = l_{TSV} * \frac{\sqrt{\pi \mu f \sigma}}{r\sigma}$

Where l_{tsv} is the length of the TSV, μ is the permeability, f is the frequency, r the radius and σ the electrical conductivity.

So, the total resistance of the TSV given by the equation:

$R_{TSV} = R_{dc} + R_{ac}$

According to observations, we notice that when radius increased, the resistance reduced. In addition to this resistance increases due to skin effect for higher diameter TSV structures.

- LTSV Model

The partial self-inductance of the TSV is given by the equation:

$L_{TSV} = (\frac{\mu lTSV}{2\pi})*[\ln(\frac{lTSV}{rm} + \sqrt{((\frac{lTSV}{rm})^2+1)} + \frac{rm}{lTSV} - \sqrt{((\frac{rm}{lTSV})^2+1)}]$

Where μ is the permeability of free space given by $4\pi \times 10^{-7}$ H/m and depends upon the diameter and length of the TSV.

According to observations, we notice that for a stable TSV length, when the radius increases, the inductance decreases. Furthermore, when the $\frac{lTSV}{rm}$ ratio is lower, the self-inductance of TSV is reduced.

- CTSV Model

The capacitance between the TSV and the silicon substrate is the most important parameter for the TSV procedure.

An analytical expression can be CTSV obtained by solving the equation Poisson 's. While the MOS flat capacitor structure has been studied analytically by solving Equation Poisson in a Cartesian coordinate system, the TSV MOS capacitor requires a solution of the Poisson's equation in a

cylindrical coordinate system. It is sufficient to solve a 1-D Poisson's equation in the radial direction, as the peripheral (Φ) and the longitudinal (z) variation in potential (Ψ) is insignificant.

The 1-D equation in cylindrical coordinates Poisson system with p-Si substrate is given by:

$(\frac{1}{r}) * (\frac{d}{dr}) * (r * \frac{d\psi}{dr}) = \frac{qN\alpha}{\varepsilon si}$

Where r is the radius, q is the electron charge, Na is the doping concentration of p-Si substrate, and ε_{si} is the permittivity of silicon.

The nature of TSV CV characteristics are similar to the planar capacitor MOS so that the accumulation capacitance is the capacitance of oxide and given as:

$C_{TSVACC} = C_{OX} = \frac{2\pi\varepsilon OXlTSV}{\ln(\frac{ROX}{RMetal})}$

The accumulation region appears when the flat voltage is bigger than the applied voltage ($V_{TSV} < V_{fb}$).

When threshold voltage is bigger than the applied voltage ($V_{fb} < V_{TSV} < V_{th}$) the majority carriers are depleted for distance from the surface to w_d. So the new capacitor given by:

$C_{TSV} = \frac{CdepCOX}{Cdep + COX}$ Where the depletion capacitance given by :

$C_{dep} = \frac{2\pi\varepsilon stltsv}{\ln(rm + tox + \frac{Wd}{rm} + tox)}$

As the TSV gate bias increases, capacity depletion acts in series with the capacity of oxide such as the effective capacitance is the series combination of the oxide and depletion capacities.

It is very important to take the MOS Capacitance effect into consideration when examining the electrostatic behavior of TSVs so as to avoid considerable errors in the relation of the applied voltage with the capacitance. In order to obtain this relationship the TSV is perceived as an ideal cylindrical MOS capacitor and the same method that is used to determine the MOS capacitance of a planar structure is used. The Poisson equation in cylindrical co-ordinates can be expressed as:

$$\frac{d^2\psi}{dr^2} + \frac{1}{r}\frac{d\psi}{dr} = -\frac{\rho}{\varepsilon_{si}} \quad (1)$$

Where,

ψ = potential

ρ = charge density

ε_{si} = dielectric constant of Si

In the full depletion approximation, the depletion layer charge is only caused by the ionized doping atoms if it is assumed that the electric charge distribution does not vary with the angle around the TSV or the axial distance due to the symmetry of the structure. As a result the Poisson equation can be written as:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\psi}{dr}\right)=-\frac{qNa}{\varepsilon_{si}} \tag{2}$$

$$\psi(r)=\frac{qNa}{2\varepsilon_{si}}\left((rm+tox+wd)^2\ln\left(\frac{rm+tox+wd}{rm+tox}\right)-\frac{(rm+tox+wd)^2-(rm+tox)^2}{2}\right) \tag{3}$$

This relation is integrated from $r_m + t_{ox}$ to $r_m + t_{ox} + w_d$

Where rm is the radius of the via, tox, the isolation dielectric thickness, and wd the width of the depletion area as well as assuming that the potential at the end of the depletion area is equal to zero. After integrating twice the result is that of the electrical potential at the Si-SiO2 interface.

It is interesting that the potential at the surface when the depletion radius is at its maximum value is:

$$\psi_s=2\ln\left(\frac{Na}{ni}\right) \tag{4}$$

Therefore by combining equations (3) and (4) we can derive the maximum radius of the depletion region.

The applied TSV voltage drops across the TSV oxide as well as the silicon substrate, as given in:

$$Vtsv=Vfb+\frac{qNa}{2\varepsilon_{si}}\left((rm+tox+wd)^2\ln\left(\frac{rm+tox+wd}{rm+tox}\right)-\frac{(rm+tox+wd)^2-(rm+tox)^2}{2}\right)+\frac{qNa\pi((rm+tox+wd)^2-(rm+tox)^2)}{Cox}$$

Where the flatband voltage is: $Vfb=\phi ms-\frac{qQeq2\pi(rm+tox)}{Cox}$

$$Cox = \frac{2\pi\varepsilon oxltsv}{\ln(\frac{rm+tox}{rn})}$$

$$Ctsv = \frac{2\pi\varepsilon ox\varepsilon siltsv}{\varepsilon ox\ln(\frac{rm+tox+wd}{rn+tox}) + \varepsilon si\ln(\frac{rm+tox}{rm})}$$

The results of mathematical models for the TSV parasitic can be seen in Table

	R_{TSV} [Ω]	L_{TSV} [pH]	C_{TSV} [pF]	R_{Si} [kΩ]
Theoretical values for TSV models	0.012	87.761	0.8642	5.8421

Table 2-1

2.3 Impedance

To study more analytically the TSV behavior, we compute the impedance of a TSV.

Firstly, we solve the equation to find the Impedance and then we plot it on Matlab. The Matlab code is presented in the Appendix and the plot given in Figure 2-3.

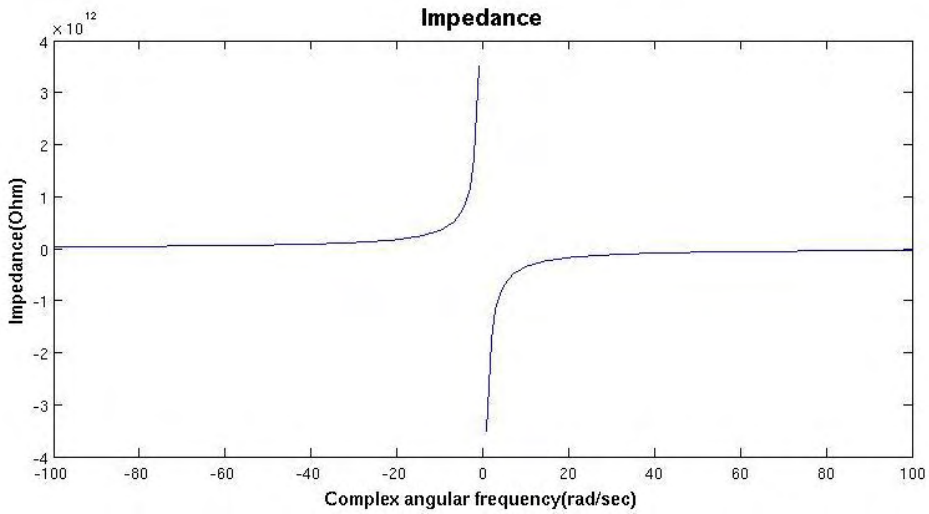


Figure 2-3 TSV impedance as a function of Complex angular frequency

2.4 TSV Models

In this section the equivalent electrical circuits for four cases are presented

(a) directly to the ground

is the ideal case where the parasitic MOS capacitor is grounded.

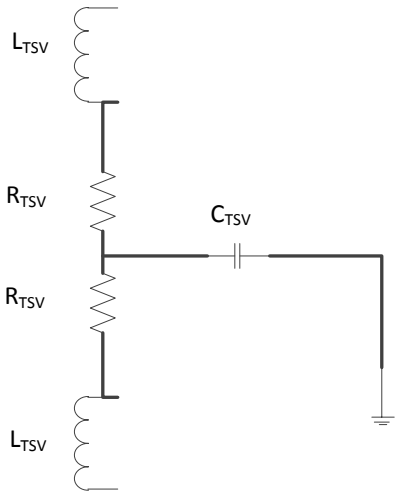


Figure 2-4 Case a

(b) to a guard ring

The TSV is coupled with the ground through a guard ring, p+ doping, over the resistive bulk.

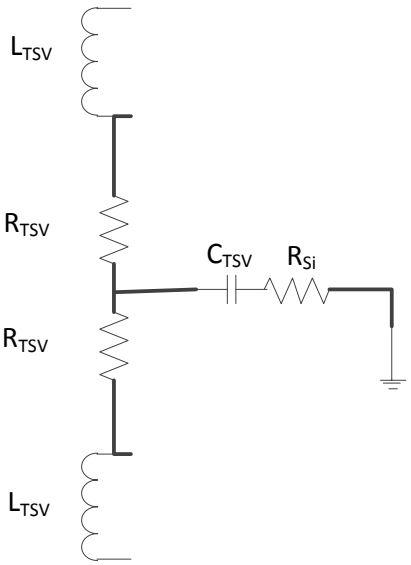


Figure 2-5 Case b

(c) to a second TSV

The TSV is coupled to a n-well over the resistive bulk and a parasitic diode

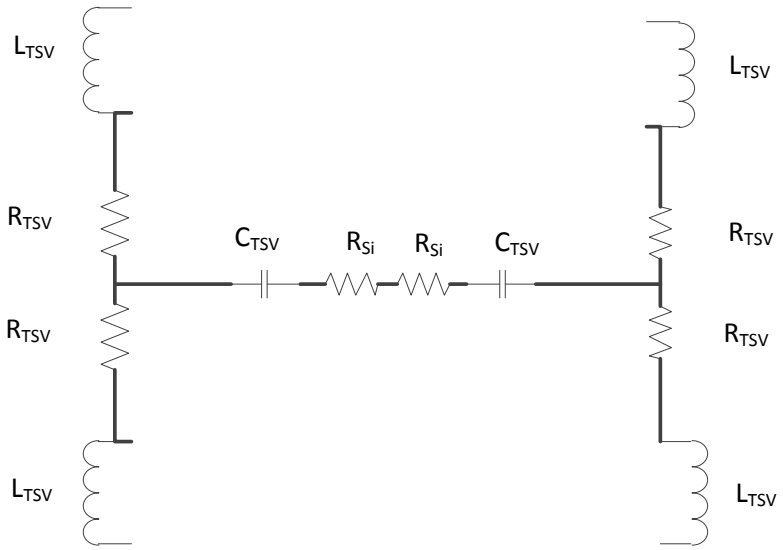


Figure 2-6 Case c

(d) to a n-well

One TSV is coupled to a second one where the coupling occurs over the TSVs mutual inductance, L_{mutual}, and through the Si bulk. The resistance of the bulk is noted as R_{si}.

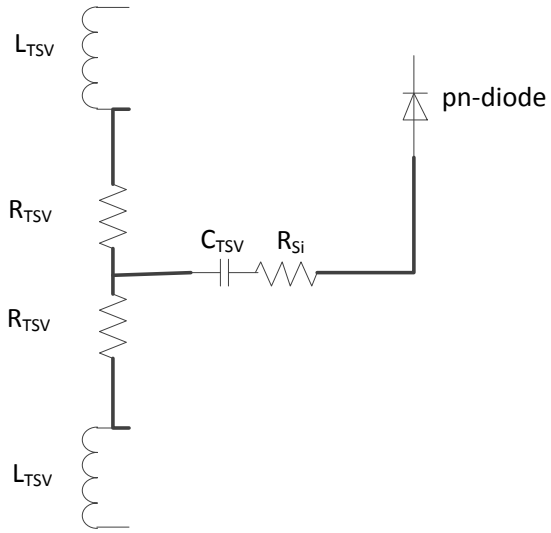


Figure 2-7 Case d

The bulk resistance is approximately given by:

$R_{si} = \frac{\rho\, d}{2\mathrm{rml}\mathrm{TSV}}$ and ρ is the resistivity of the bulk.

(e) Proposed model including leakage resistors for C_{ox} and C_{dep}

In this model the depletion capacitance is in series with the oxide capacitance. Parallel to the two capacitors, two resistors can be placed to model their leakage

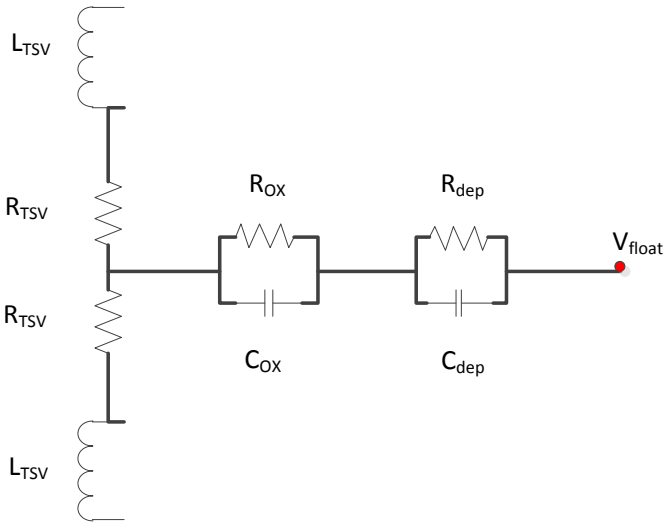


Figure 2-8 Case e

2.5 TIMING ANALYSIS FOR DIFFERENT COUPLING SCENARIOS

Using the cross-talk models that we discussed before, we study delay times and the voltage difference of the two nodes of the parasitic MOS. The voltage difference was investigated for the rise and fall of a square pulse.

Two buffers were used to drive the TSV and another two buffers where used on the other side to emulate a signal regeneration scheme.

The cross-talk of two TSVs is studied for three cases

(a) the second TSV is connected to the ground,

(b) the second TSV is connected to the VDD and

(c) the second TSV is carrying the same signal.

The worst delay occurs in the case of two TSVs where one of them carries a signal and the other one is connected to VDD (case (b)). The delay measured was 2.03ns.The best case is for two TSVs both

carrying the same signal (case (c)). The delay in this case was 17.01ps. All other cases provide intermediate results. The results are presented in Table

Case	Name	Delay	d V max	d V fall	d V rise	More negative V value
a	Single TSV	67.17E-12	1 V	-	1 V	- 0.01 V (VCin)
b	Single TSV with Rsub	48.84E-12	0.82 V	1.38 V	0.82 V	- 0.37 V (VCout)
C1	Two TSVs with Rsub(the 2nd with VDD)	2.032E-9	0.5 V	0 V	0 V	- 0.015 V (VCin)
C2	Two TSVs with Rsub(the 2nd with GND)	32.36E-12	0.5 V	0.5 V	0.5 V	- 0.02 V (VCout)
C3	Two TSVs with Rsub(the 2nd with Buffer)	17.01E-12	0.4 V	0.4 V	0.4 V	- 0.03 V (VCin)
d	Single TSV with Rsub connected to diode	21.22E-12	0.53 V	0.75 V	0.53 V	- 0.24 V (VCout)

Table 2-2 TSV Design Perturbation, introducing process variability effects

The Rsub introduces a voltage drop on one node of the MOS that reduces the voltage across it. What is most interesting is that for the falling edge of the pulse, for a short time the MOS capacitor is negative biased. That negative bias for the test case studied here is -300mV. In the case of noise in the pulse then the aforementioned voltage can be dropped to more negative values, which may cause problem to the system since if it gets bellow the V_{th} the MOS capacitance can increase sharply. The results of timing analysis for the six different scenarios can be seen in the Figures 2-9 – 2-20.

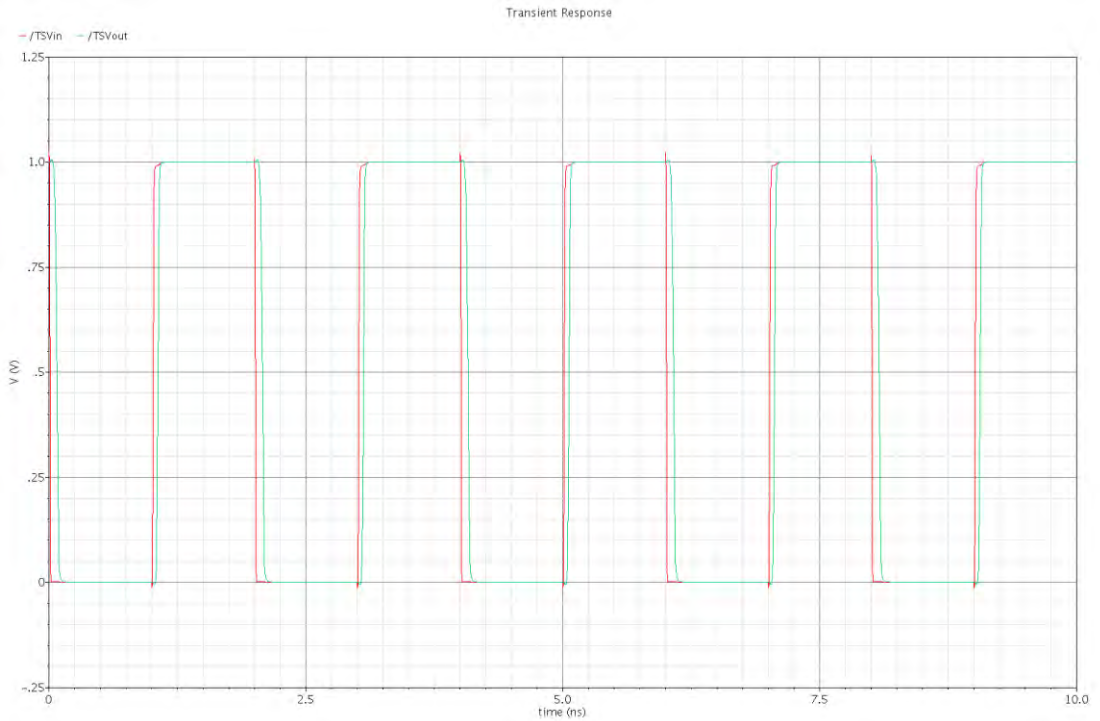


Figure 2-9 Transient analysis with stop time 10ns for the Voltage at TSV input and output as a function of time – case a

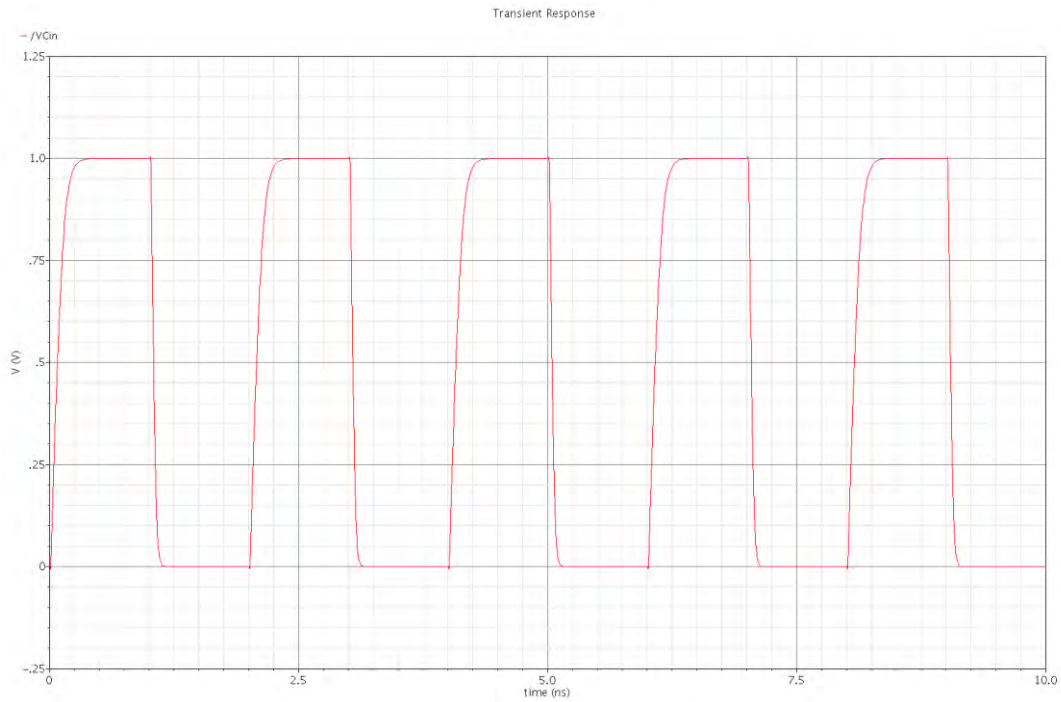


Figure 2-10 Transient analysis with stop time 10ns for the Voltage at C_{TSV} input and output as a function of time – case a

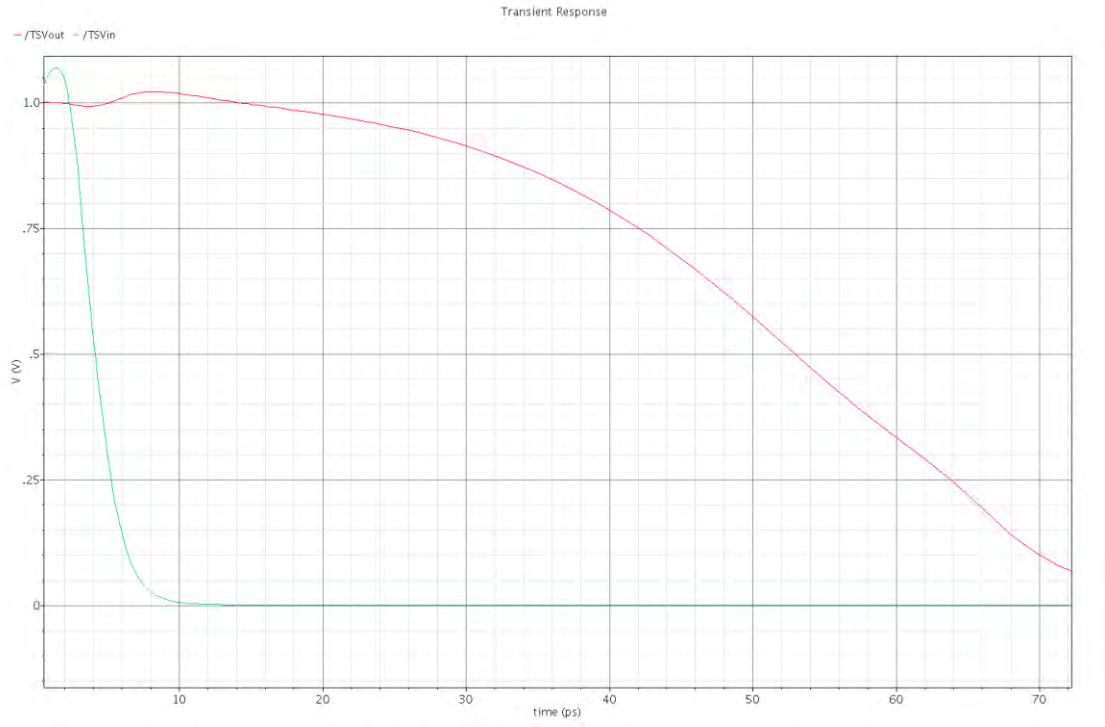


Figure 2-11 Transient analysis with stop time 10ns for the Voltage at TSV input and output as a function of time – case b

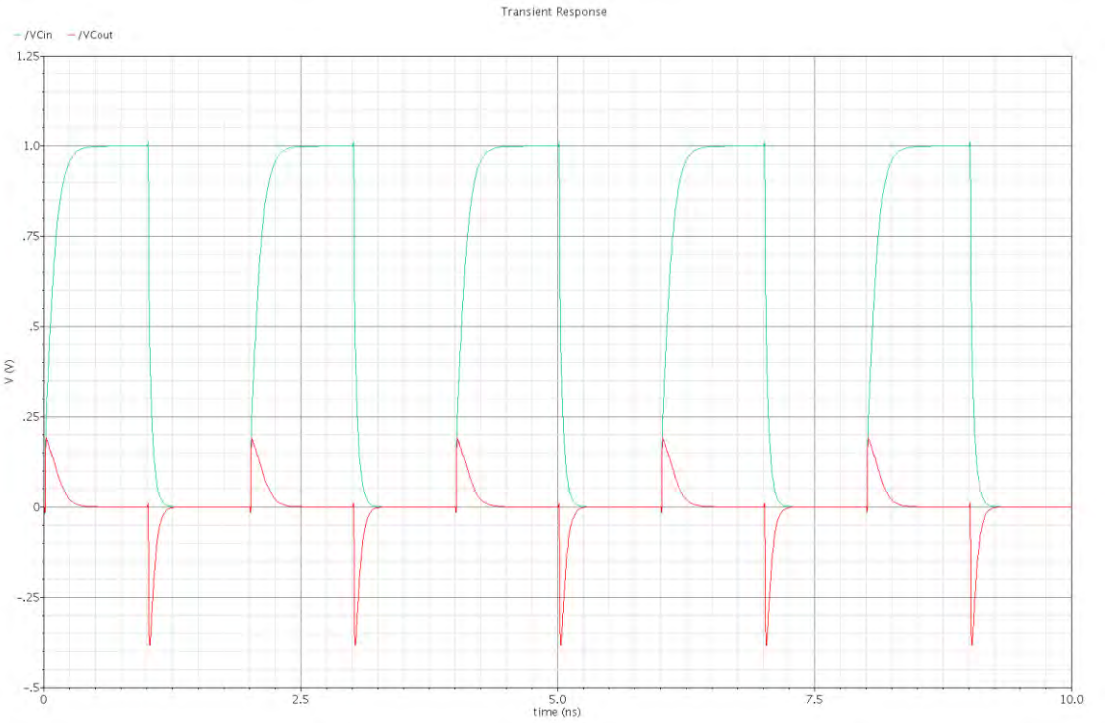


Figure 2-12 Transient analysis with stop time 10ns for the Voltage at C_{TSV} input and output as a function of time – case b

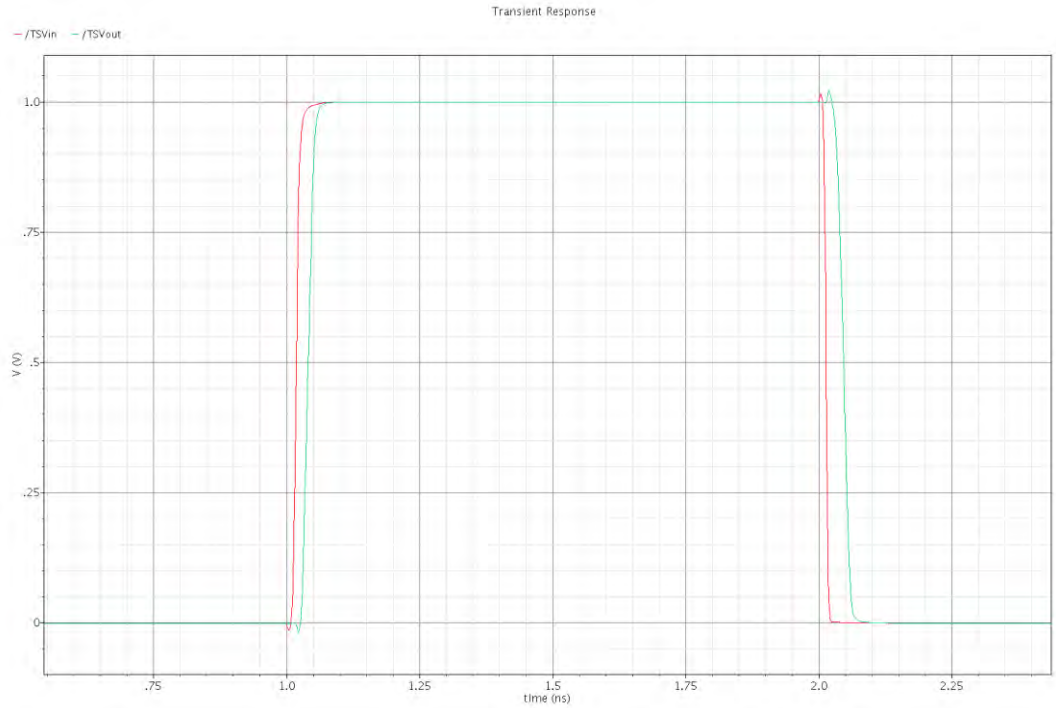


Figure 2-13 Transient analysis with stop time 10ns for the Voltage at TSV input and output as a function of time – case c1

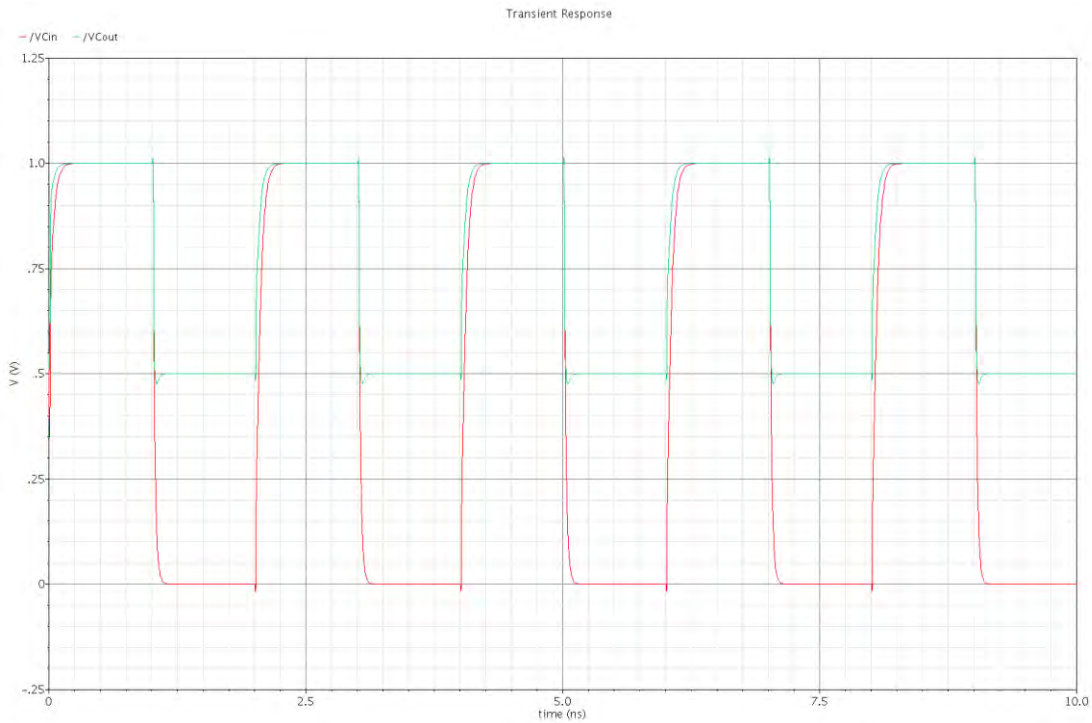


Figure 2-14 Transient analysis with stop time 10ns for the Voltage at C_{TSV} input and output as a function of time – case c1

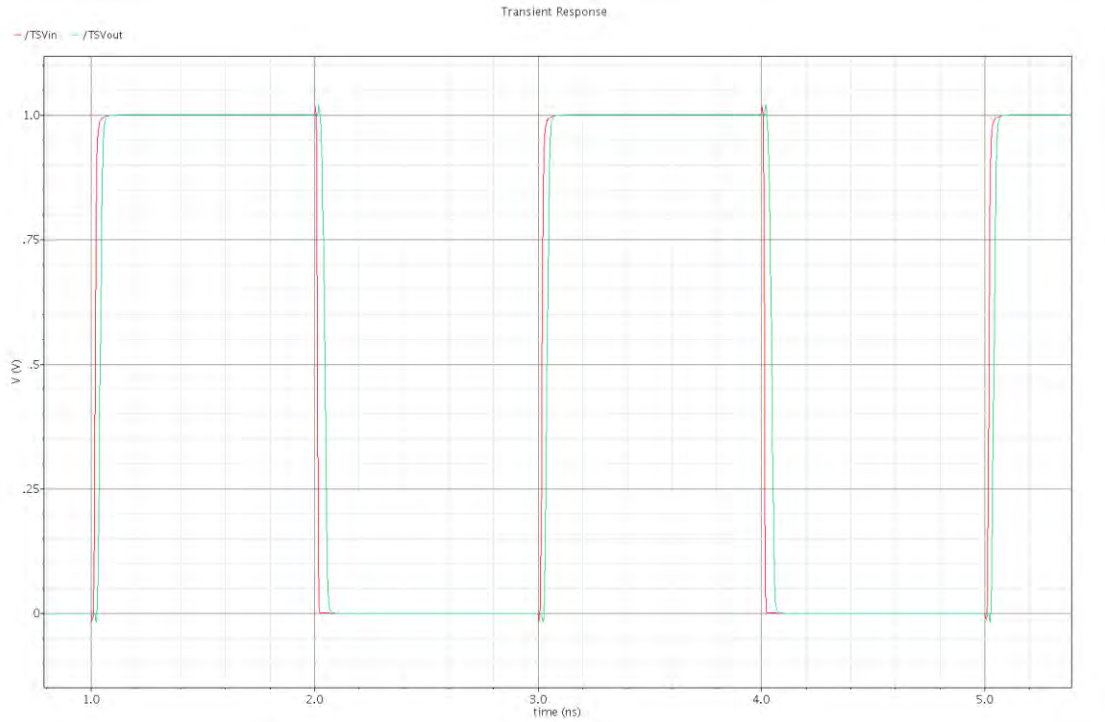


Figure 2-15 Transient analysis with stop time 10ns for the Voltage at TSV input and output as a function of time – case c2

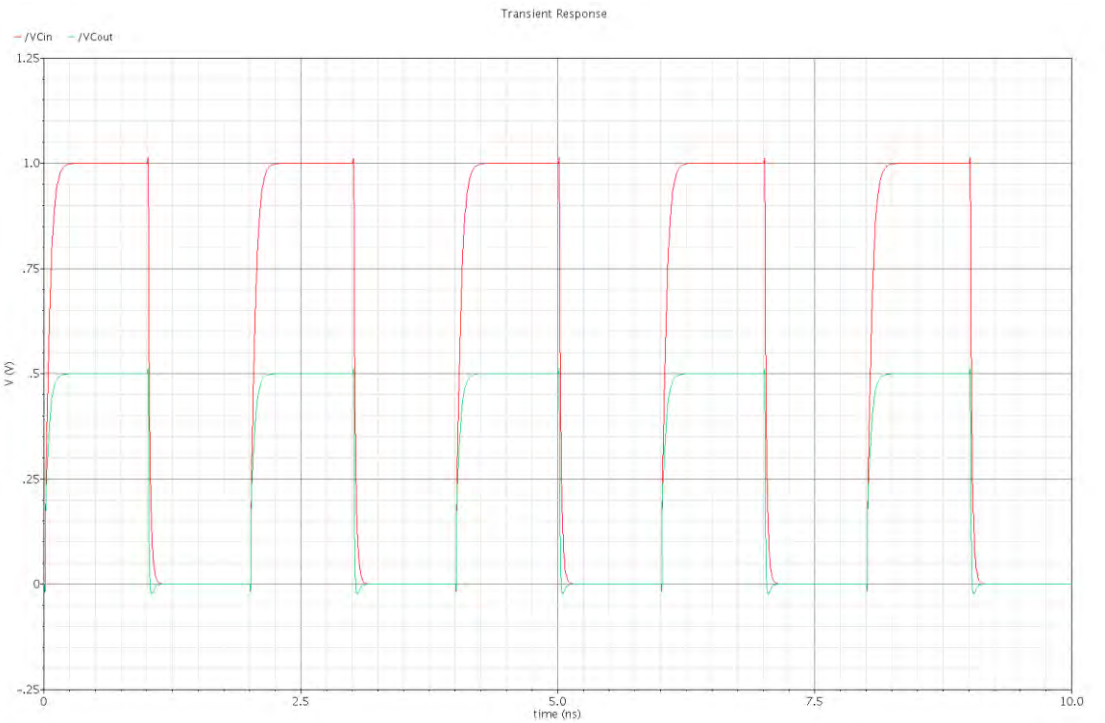


Figure 2-16 Transient analysis with stop time 10ns for the Voltage at C_{TSV} input and output as a function of time – case c2

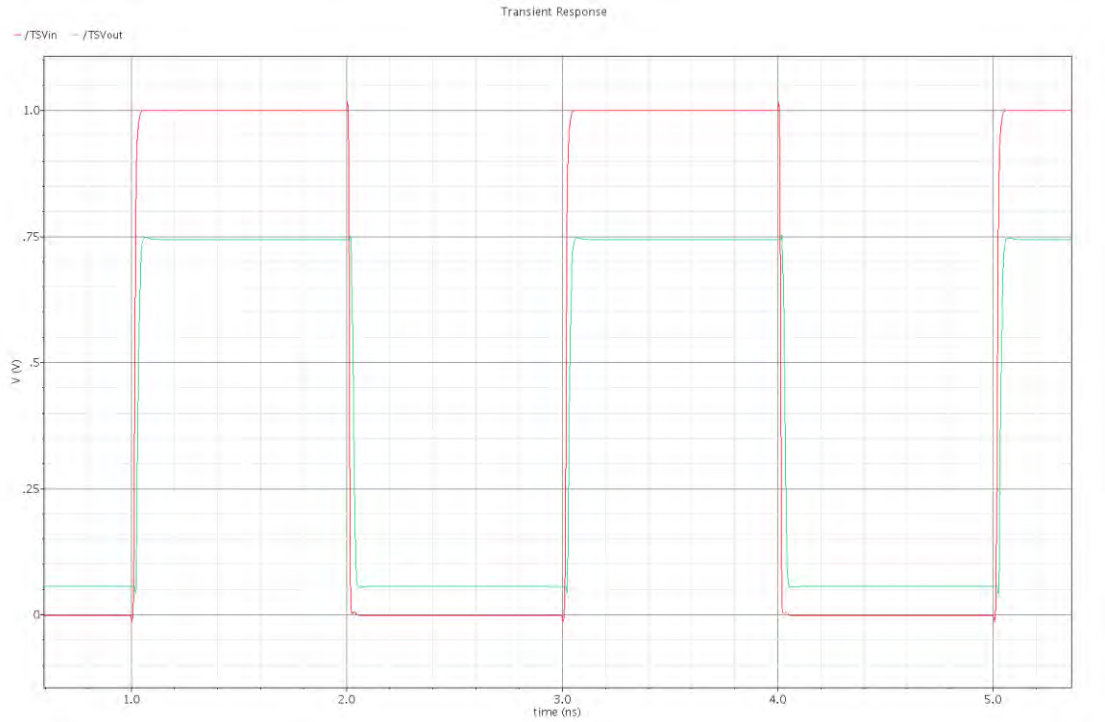


Figure 2-17 Transient analysis with stop time 10ns for the Voltage at TSV input and output as a function of time – case c3

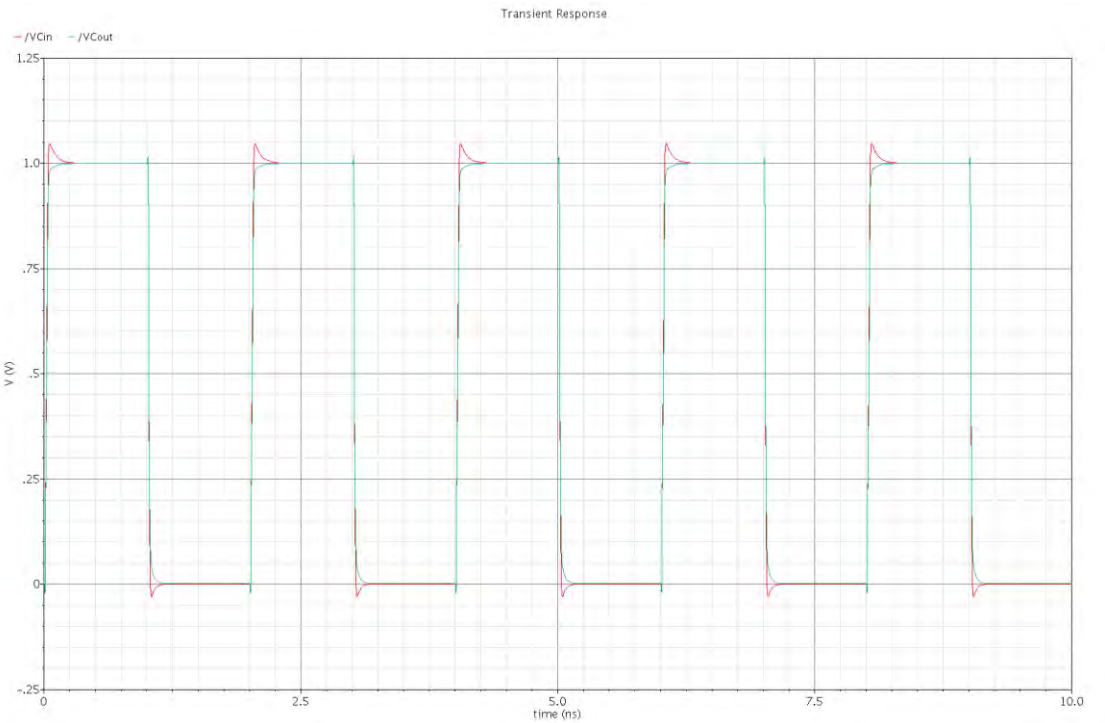


Figure 2-18 Transient analysis with stop time 10ns for the Voltage at C_{TSV} input and output as a function of time – case c3

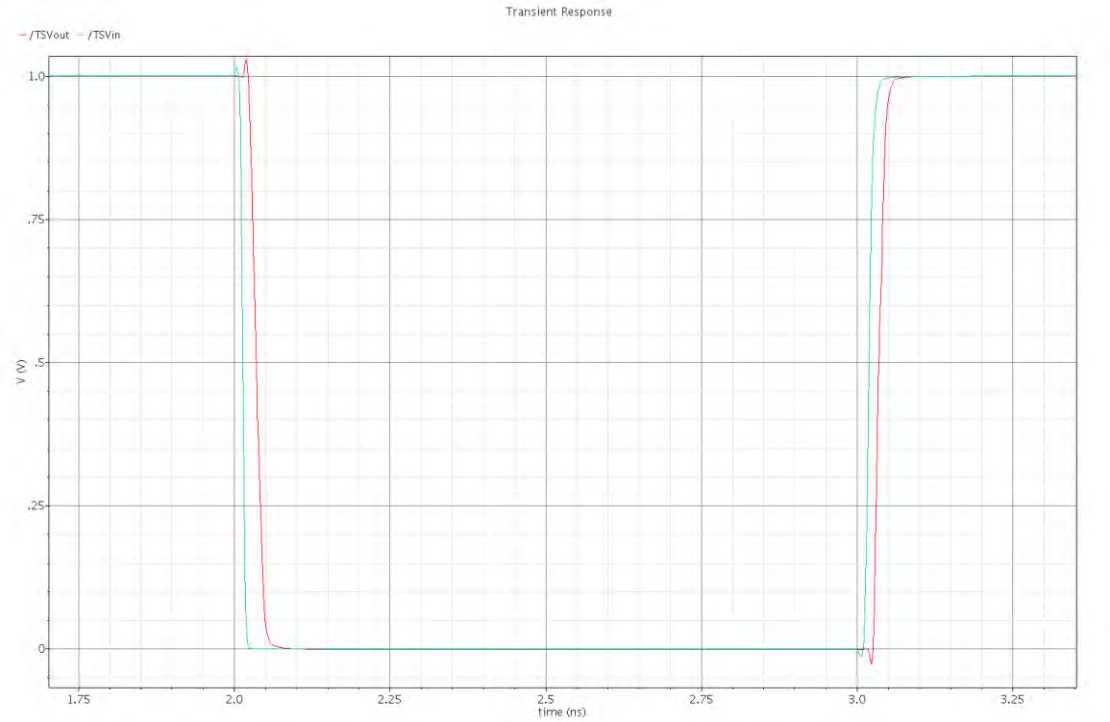


Figure 2-19 Transient analysis with stop time 10ns for the Voltage at TSV input and output as a function of time – case d

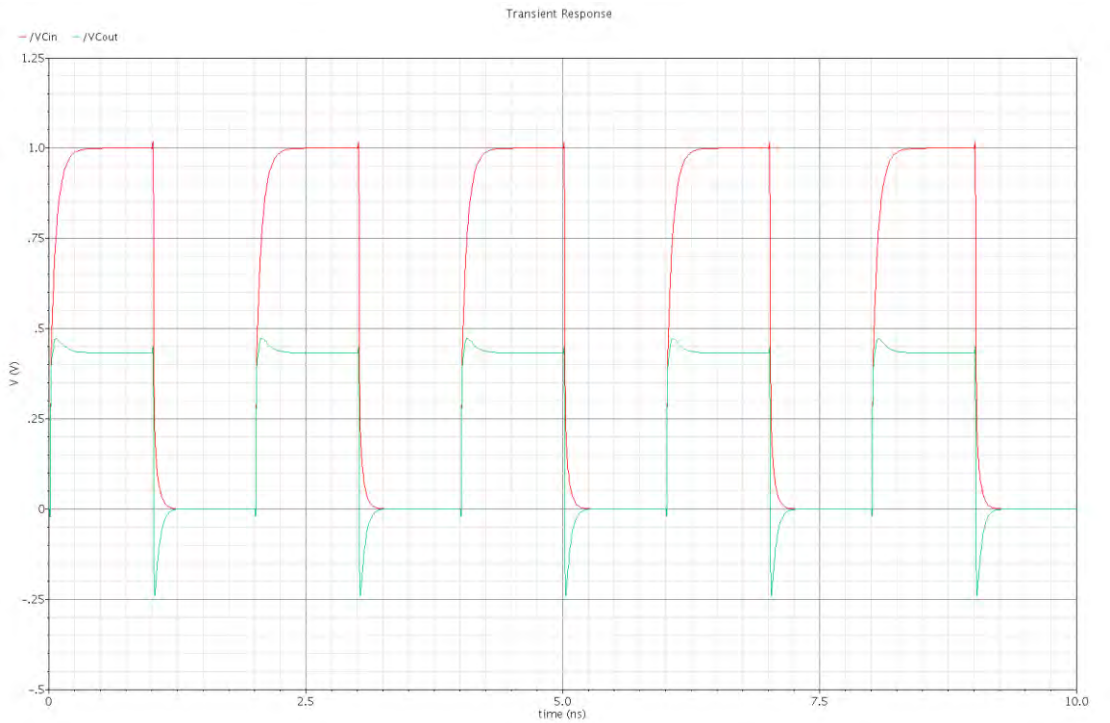


Figure 2-20 Transient analysis with stop time 10ns for the Voltage at C_{TSV} input and output as a function of time – case d

Chapter 3. RF Measurements

In this chapter Radiofrequency TSV measurements will be discussed. More particularly, the TSVs consist of parasitics and also from a MOS-capacitor whose value is critical to measure since it can affect significantly the overall emulation of the behavior of a TSV. Many mathematical models have attempted to calculate this value.

The first section will describe the RF measurement procedure and also the equipment used. Afterwards the measurement results will be presented in the form of histograms. Additionally, the aim of this chapter is on the one hand to validate the value of MOS-capacitor extracted by theoretical mathematic models with the experimental measurements and from the other hand to find the proper value for MOS-capacitor to demonstrate their behavior. Extracting the correct value of MOS-capacitor can be the beginning for TSV model expansion in the future.

3.1 The TSV measurement procedure

For the AC radiofrequency (RF) measurements a Cascade Microtech RF Probe Station was used which was connected to a HP 4284A RLC meter. For the measurements coaxial needles we opted for the smallest and most sensitive. We must underline that these needles have parasitics that can affect the measure values if the option "correction OFF" in the HP 4285A RLC meter is selected. Otherwise, with "correction ON", the parasitics from the needles are insignificant. During the setup of the RLC meter, the cable length and a number of samples were taken into account as well. For the measurements both open and short corrections were used. For open corrections the needles were placed at a measuring distance of 8 TSVs and were not in contact with the wafer and for short corrections both of the needles landed on the same TSV.

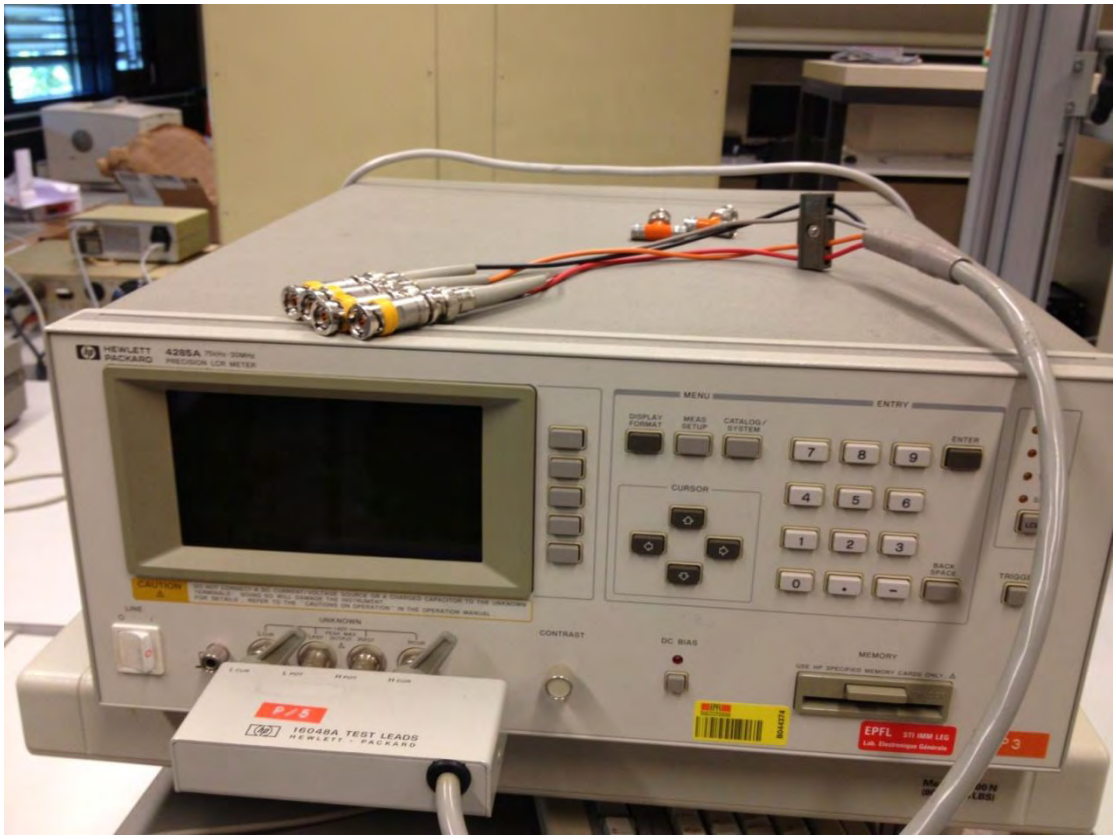


Figure 3-1 HP 4285A RLC meter

Concerning the Cascade Microtech RF Probe Station (Fig. 3.2) being very useful and very important equipment in our attempt to measure the TSV values, it was also very sensitive so it required a lot of care and attention.

Generally speaking, a probe station is a microscope, connected with a computer and through specific software called Nucleus we can have access to it.

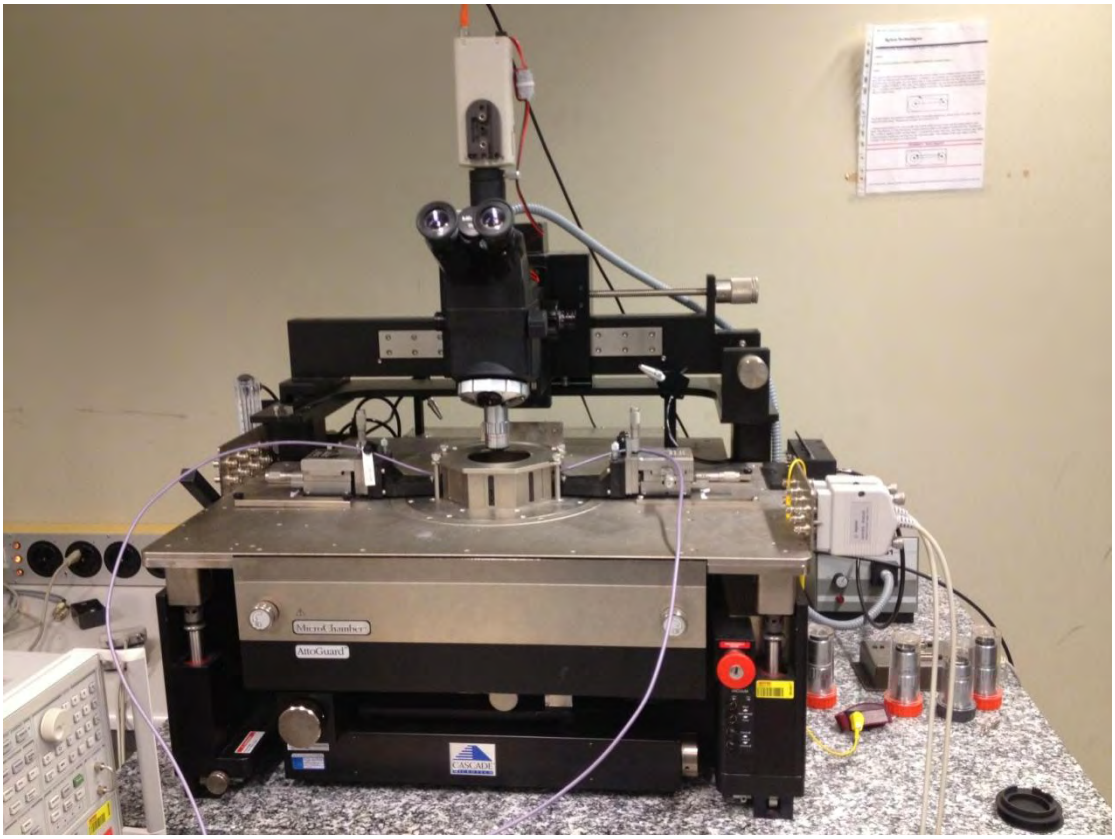


Figure 3-2 The cascade probe station

The camera and microscope are on a counterbalanced sliding rack. When we first start setting up at the probe station they will probably be raised up as high above the stage as they go. When we have our probes in the general place we expect to want them, just smoothly slide the microscope down, making sure none of the objectives bash into probes or anything else on their way down. Then whenever we need access to the area under the microscope again, just slide it back up out of the way. We must leave it up when we're finished, turn on the probe station (right side), the lamp power source (on the air table) and set the lamp intensity (small box with a knob, on the air table or the rack) to 1/2 power or higher. Finally, log on to the computer and start Nucleus. On the top menu bar, we must turn on the auxiliary power, which is the plug and socket icon (this is the power source for the camera). Also we turn on the lamp with the light bulb icon if it's not already on. The camera icon brings up the camera view. In this window we should now see whatever the microscope is focused on. On the left side another menu of icons contains an icon that will bring the stage out to the loading position.

In short, the procedure to load the wafer into the probe is:

1. Firstly, we must clean the wafer that we use for the measurements with compressed air. Even if the wafer has dust scraps, this can affect the results.
2. From the Nucleus software installed into the laboratory's computer press the button “Wafer load”.
3. Open the probe drawer and put the wafer carefully.
4. Turn the chuck vacuum on with pressing the button “Turn on the chuck vacuum”. The air gap which created keeps the wafer stable.
5. Close the probe drawer.
6. Put the wafer in the center, under the microscope, with the button “center”.
7. Turn on the microscope lamp with the button “Microscope lamp”.
8. Move the stage to separate with the button “Move the z stage to separate”(click the button twice) to stand up the wafer in the correct position. The aim of this step is the coaxial needles to touch the TSV so that the measurements can commence.

The TSVs should be visible very clearly by now.

Additionally, we can control the needles to put them into the points on TSV we want to measure. This could be made with the needle controller. We can manage the needle's position above the TSV to change the x and y coordinates. Furthermore the probe station can be operated with the aid of a joystick that you can be used to manage the wafer position.

The test chips used for validation were fully filled copper TSV. The TSV radius was 30μm, the insulator material was thermally grown SiO2 with thickness equal to 3μm and TSV height was 380μm. The dimension of the metal strip connecting the TSVs was 120μm°40μm°700nm. The distance between two TSVs was 200μm. The physical model of a TSV is shown in Fig.3-3 and a microscopy image of a cross section and (bottom) top view of the test chip is shown in Fig.3-4

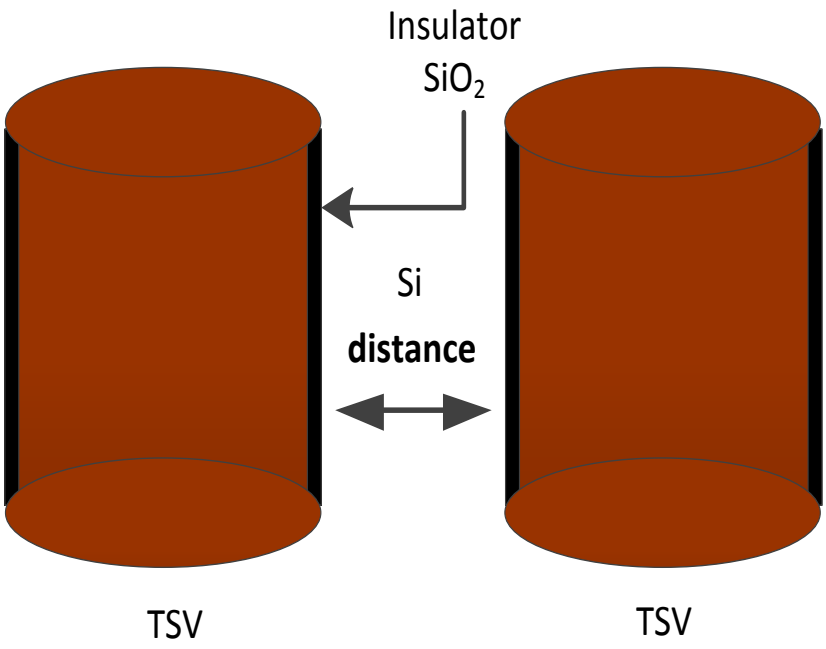
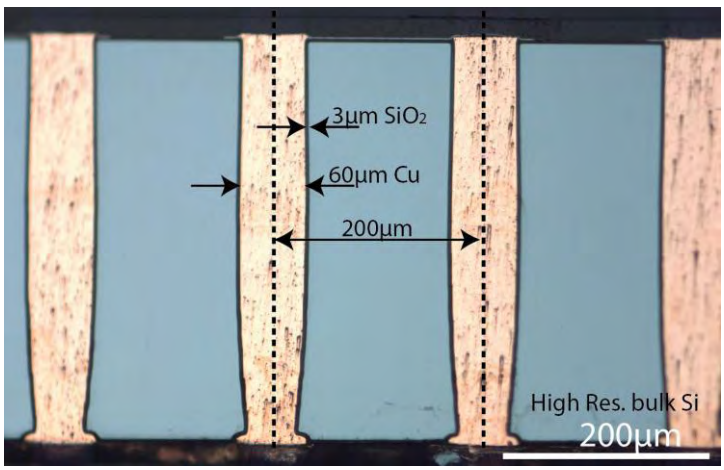
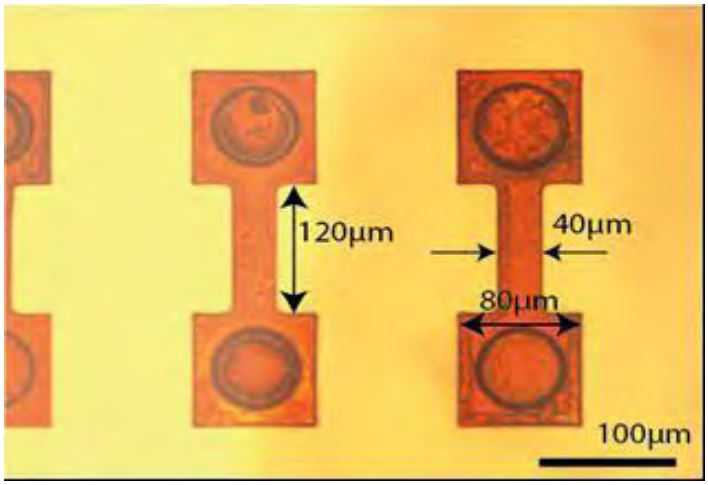


Figure 3-3 Physical model of two TSVs connected



(a)



(b)

Figure 3-4 Cross chain of the TSVs in a daisy chain (a) and Cross section of the metal lines connecting the TSVs (b)

3.2 First measurement row: Three frequencies

Our first effort was to calculate the impedance and the phase of TSVs in three different frequencies, 1MHz, 10MHz, 20MHz with V=25mV in D2 part of chip (Fig.3-15). For these measurements we used 8 TSVs connected in a daisy chain. In total 100 measurement points per frequency were collected. The results of the measurement process can be seen in the Table1 and Table2 of the appendix.

The data (detailed measurements in Appendix) is presented as histograms in Fig.3-5 – 3-6.

In Figures we can see some of the histograms but all histograms are presented in Appendix.

For comparison, the values used for the model elements are the same with the values presented in Table. If we compare our results with the mean measurements results it appears that they are close to the smaller measurements. Also capacitors of 8pf used for this match. So, these measurements assured that this model is close to reality.

Histogram for Impedance

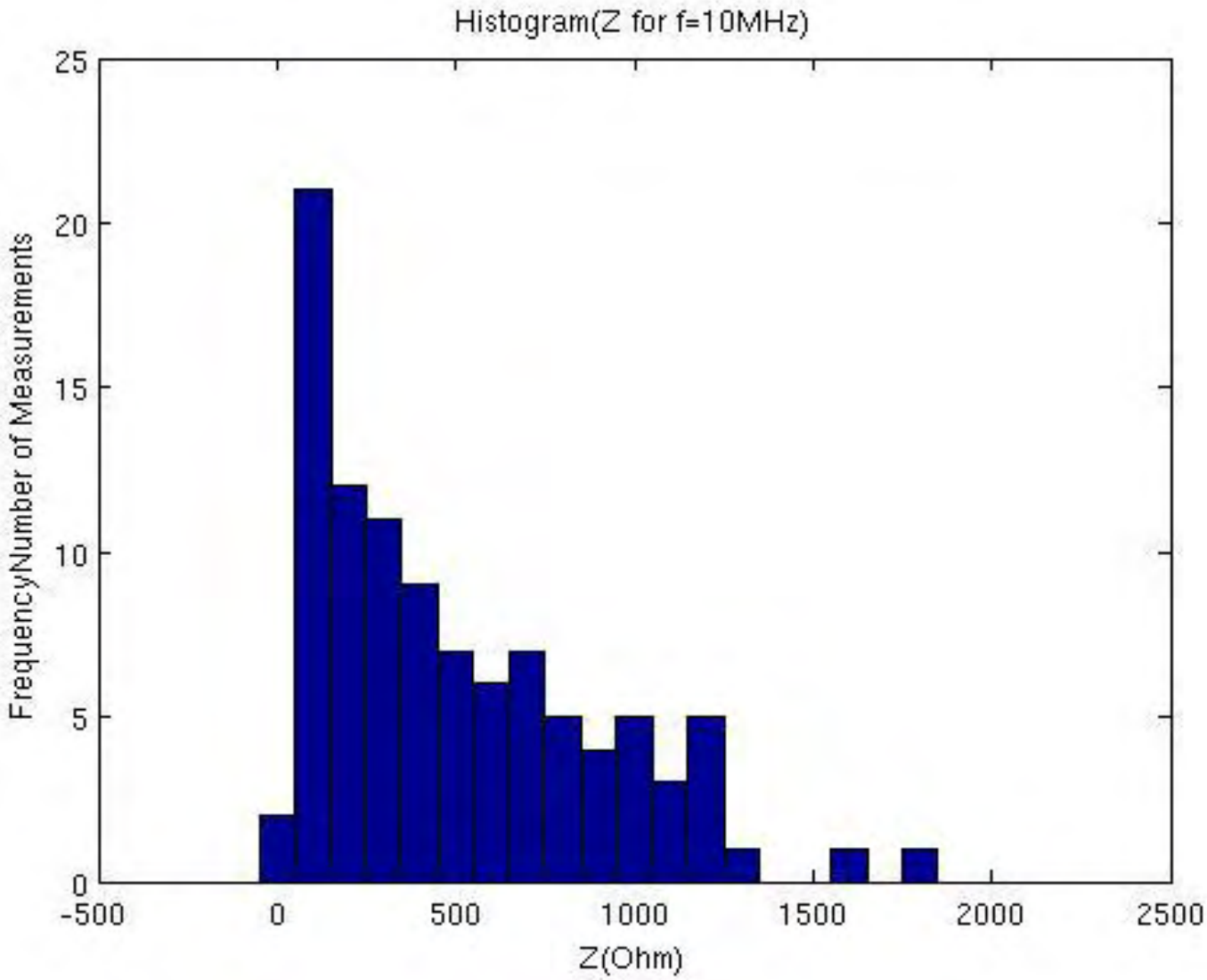


Figure 3-5

Histogram for Theta

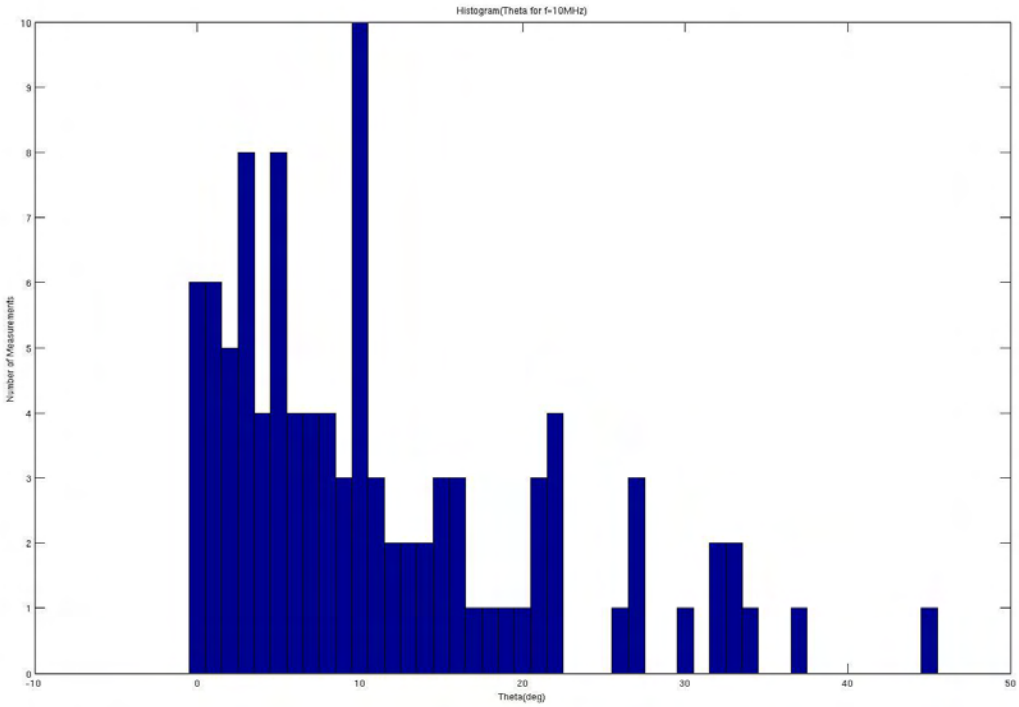


Figure 3-6

At this point it is important to note that when the frequency increases, then the inductance decreases and the phase increases. In order to be more accurate with the values of our measurements we must take into account only the measurements from the undamaged TSVs. Wrong values of measurements in the presence of damaged TSVs are common and should be tackled properly because of their significant impact. Additionally, the distance between the coaxial needles and the wafer is an important factor to achieve good measurements.

3.3 Second measurement row: 20 frequencies

Our second effort was to calculate the impedance and the phase of TSVs in twenty different frequencies, 100KHz, 150KHz, 200KHz, 250KHz, 300KHz, 350KHz, 400KHz, 450KHz, 500KHz, 550KHz, 600KHz, 650KHz, 700KHz, 800KHz, 900KHz, 1MHz, 10MHz, 15MHz, 20MHz, 30MHz with V=30mV in the C2 part of chip (Fig.3-15). For these measurements we used 8 TSVs connected in a daisy chain. In total 19 TSVs measured for each frequency. The results of the measurement process can be seen in the Table3 and Table4 of the Appendix.

The data of the tables in the Appendix are presented as histograms in fig.3-7 – 3-12.

All the histograms are in the Appendix.

For Impedance

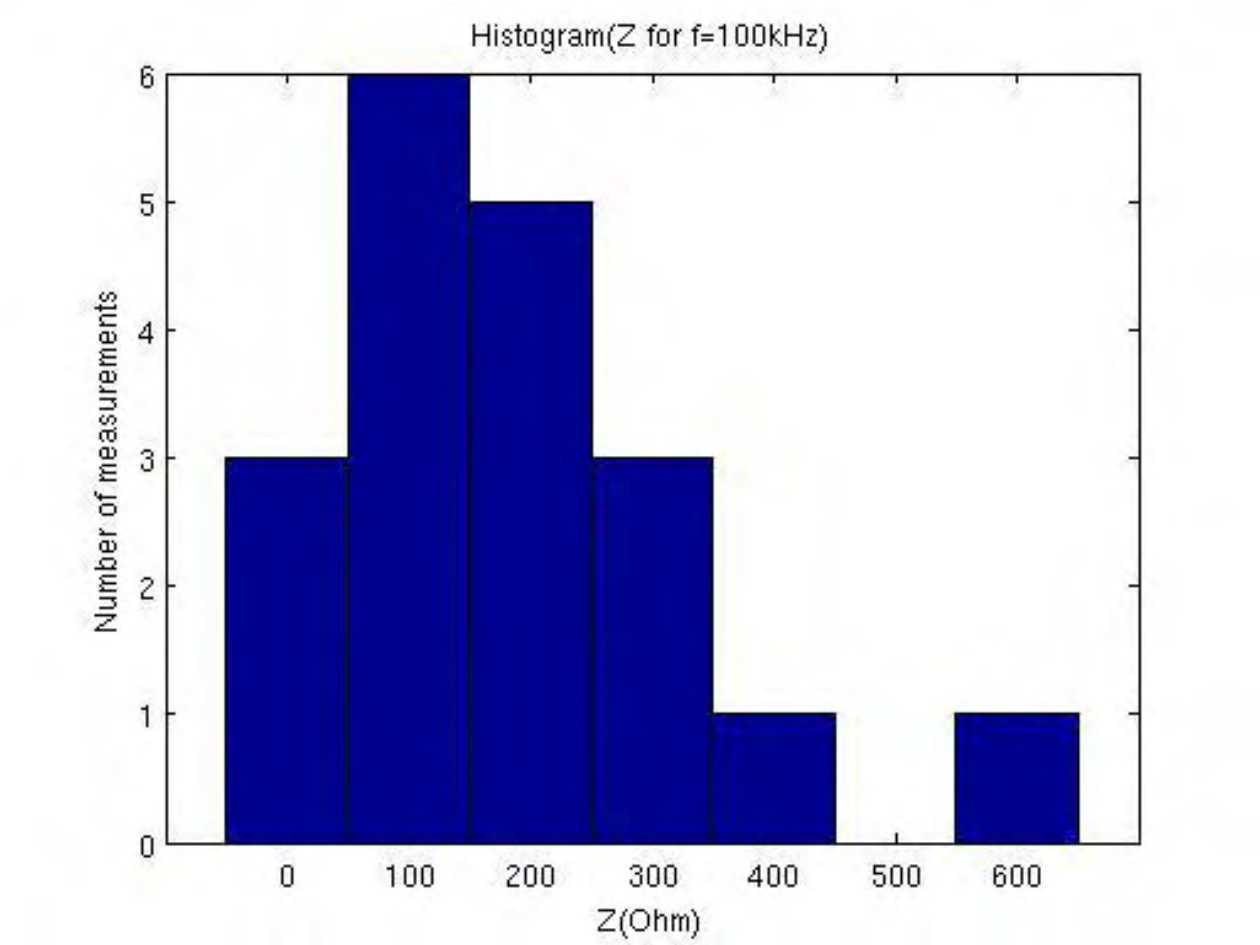


Figure 3-7

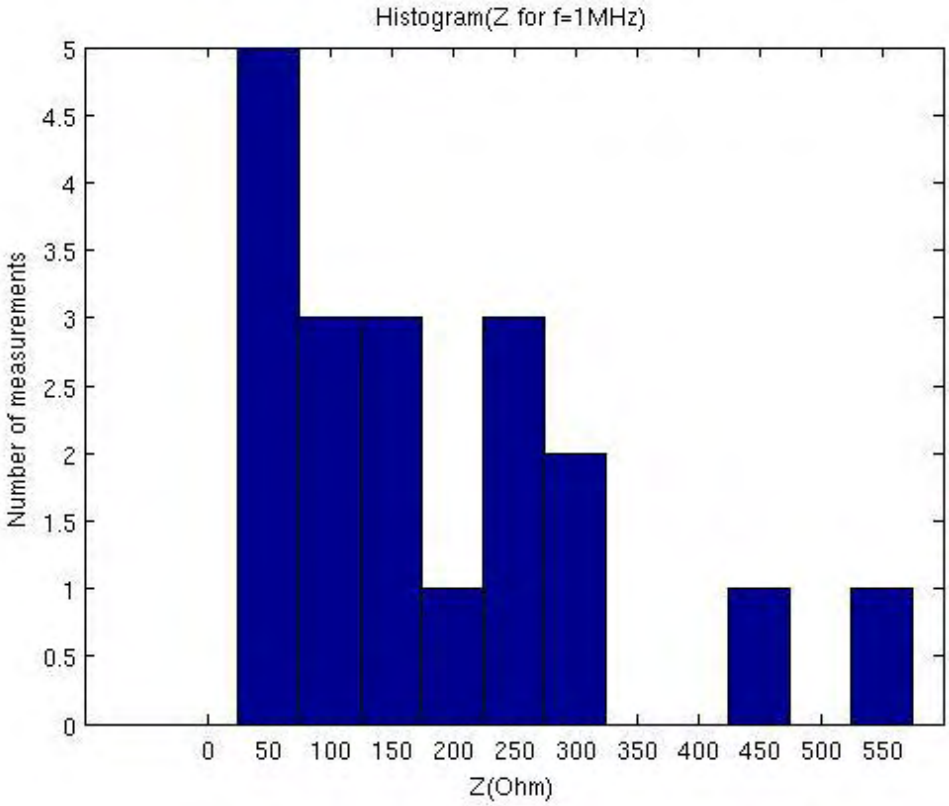


Figure 3-8

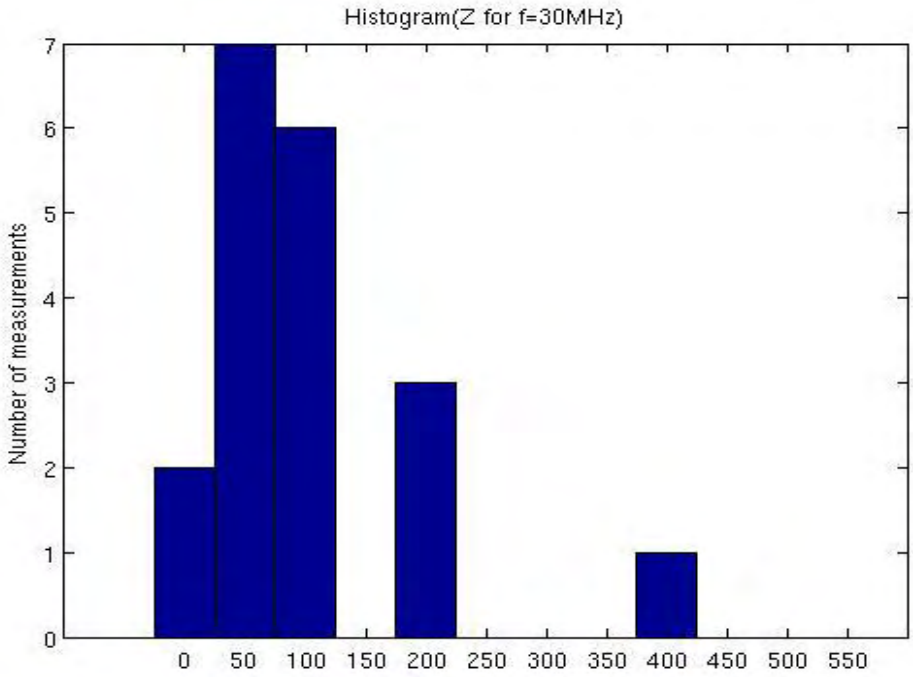


Figure 3-9

At this point it is important to underline that the histograms for the frequencies 250,300,350,400,450,500,550,600,700,800,900 KHz is almost identical because of the same values of inductance in these frequencies. The most important change of measurement values is observed in the highest frequencies like 1, 10, 15, 20, 30 Mhz, in other words in the range of MHz.

For Theta

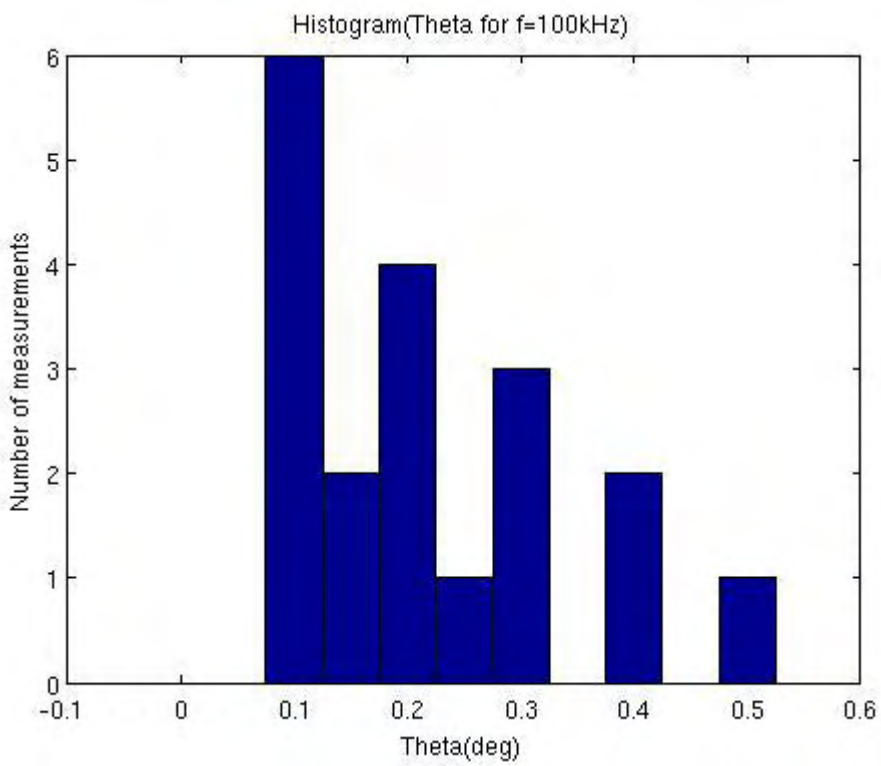


Figure 3-10

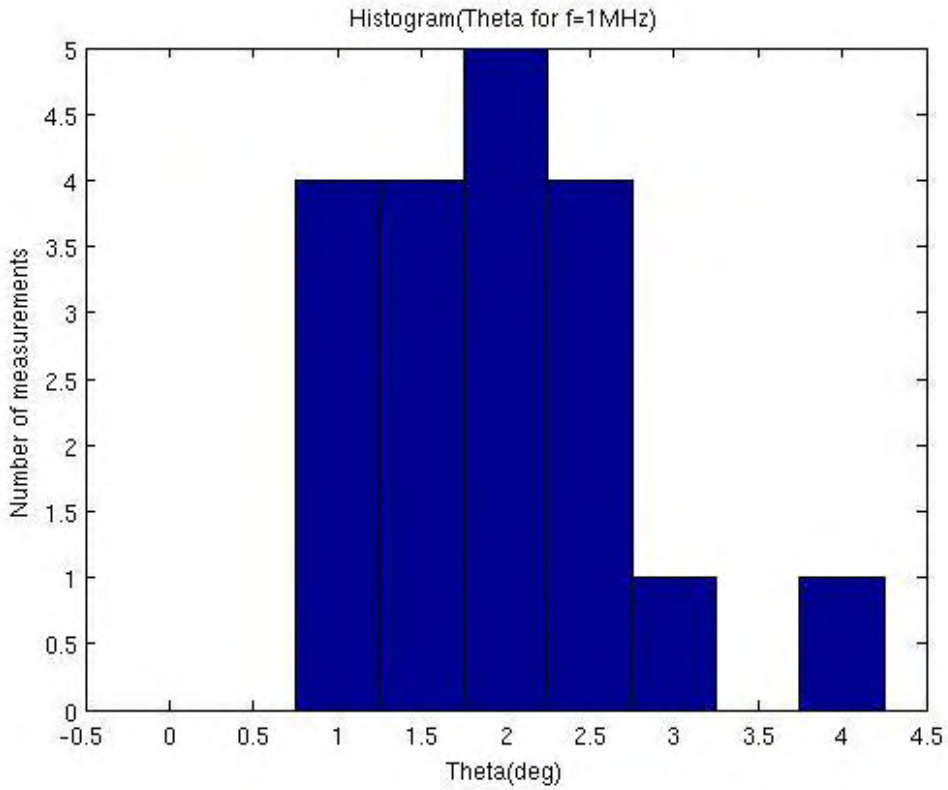


Figure 3-11

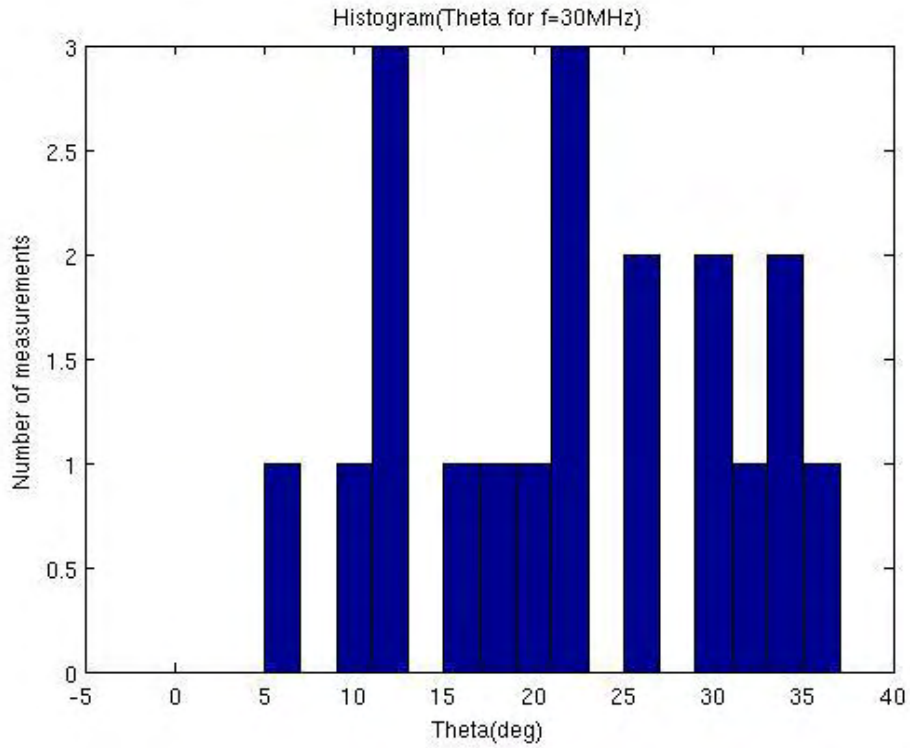
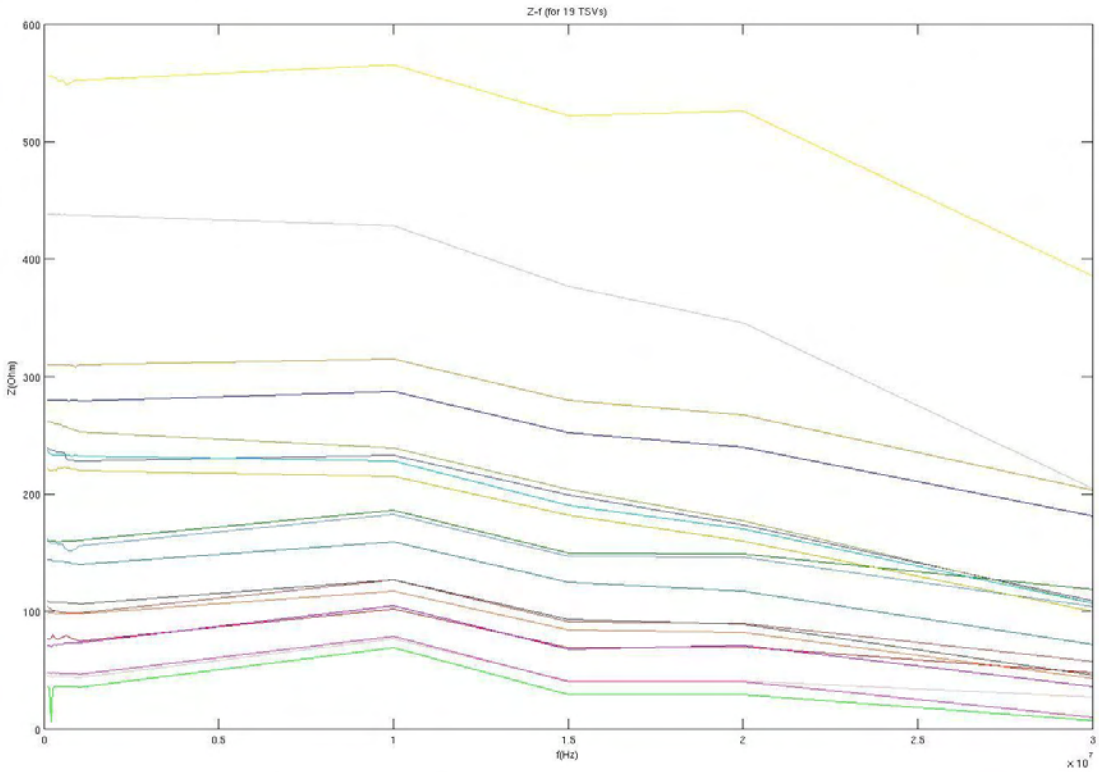


Figure 3-12

We note that when the frequency increases, then the inductance decreases and the phase increase. In the range of Mhz we notice the larger decrease of inductance and the larger increase of phase. In order to be more accurate with the values of our measurements we must take once again into account only the measurements from the undamaged TSVs.

Finally, to gain a good understanding of TSVs behavior we found the relationship between Theta-f and Z-f. The results can be seen in the Fig.3-13 – 3.14, before and after fitting.



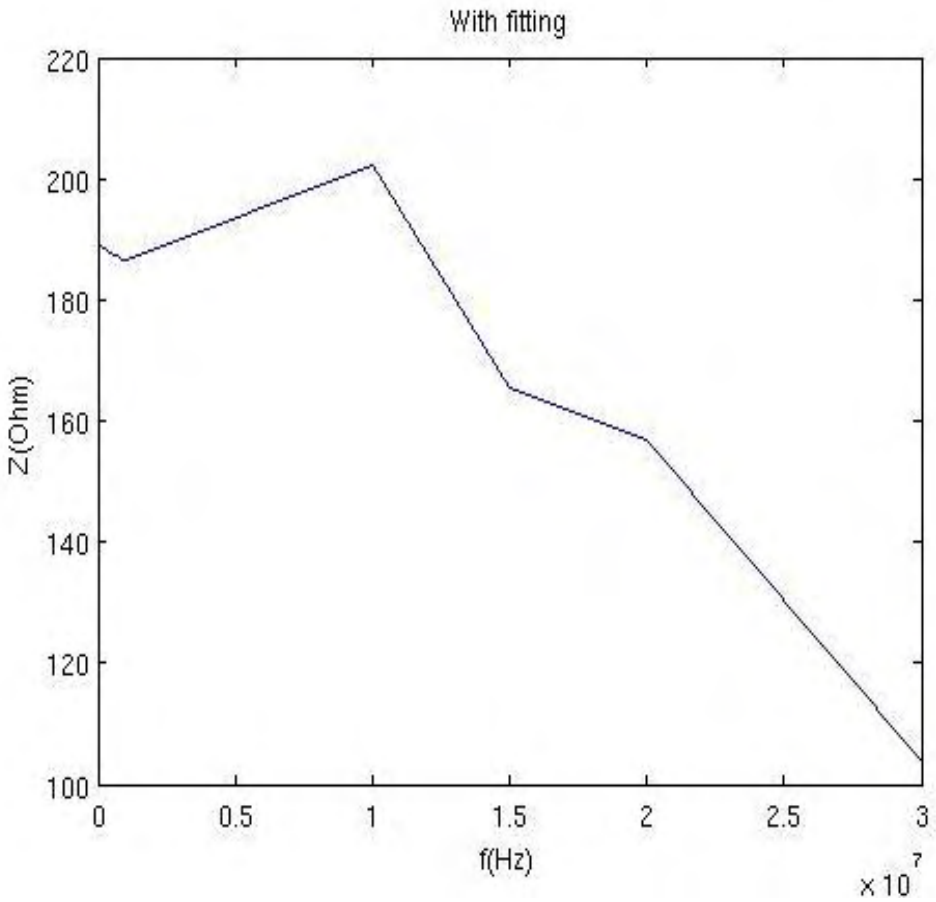


Figure 3-13 Z as a function of the frequency

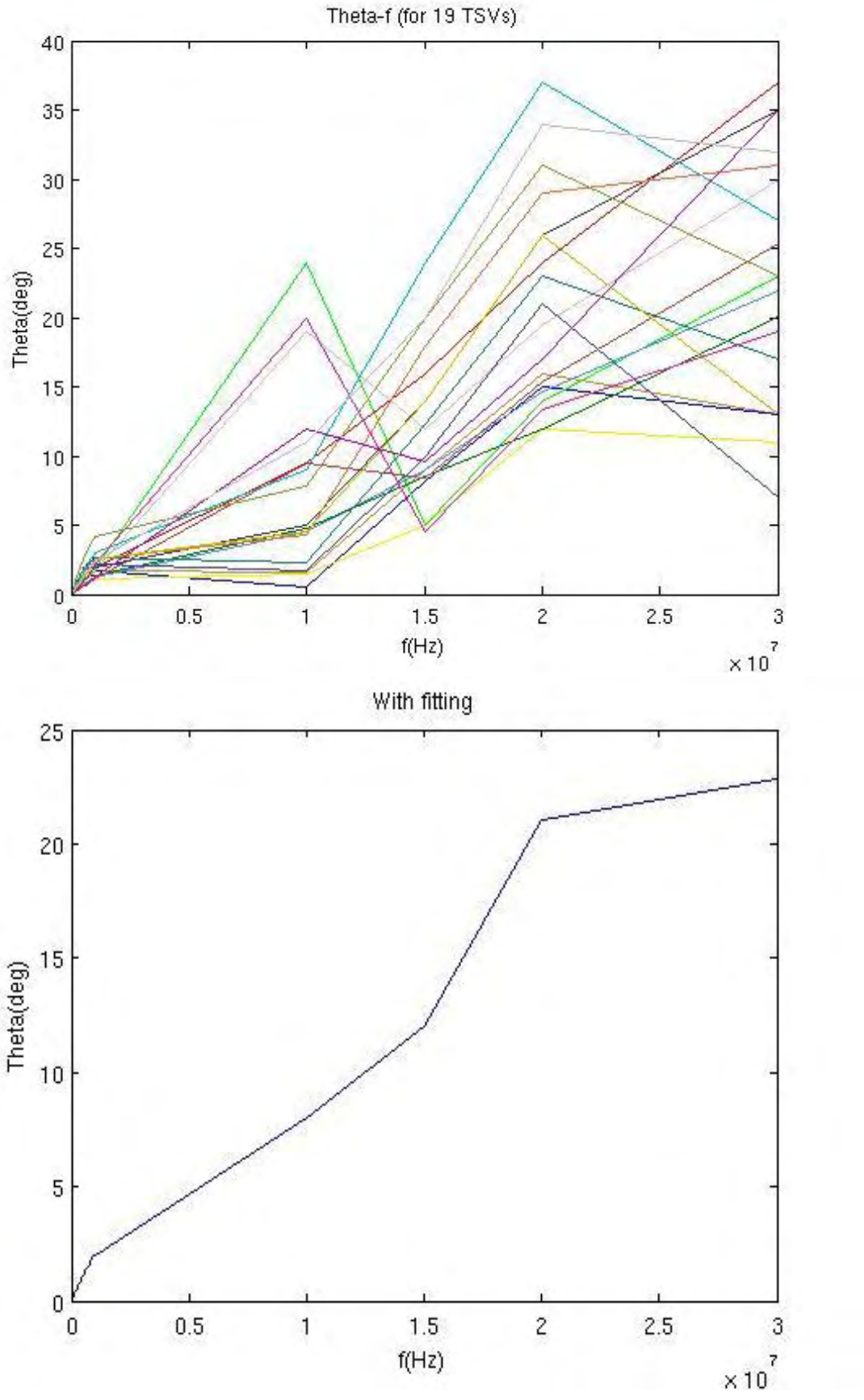


Figure 3-14 Theta as a function of the frequency

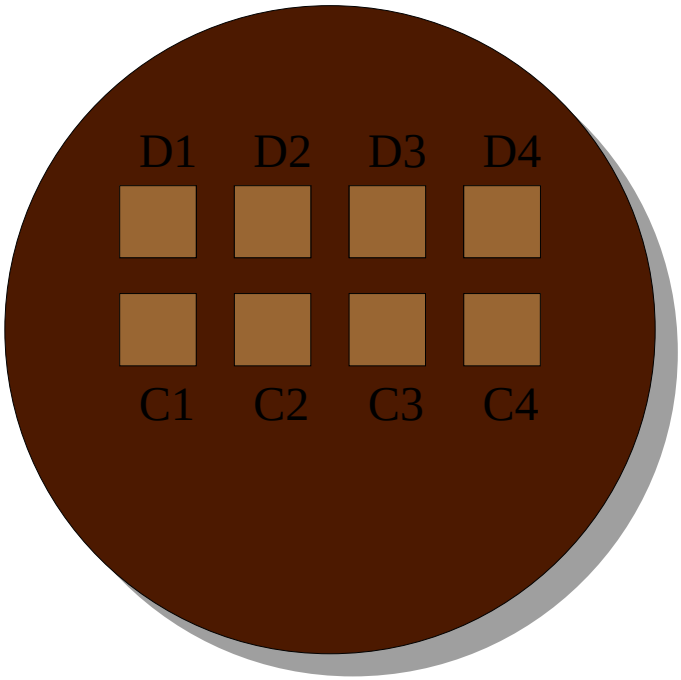


Figure 3-15 A wafer with parts C,D which contains TSVs

Chapter 4. Cad-tool to automatically convert .cir to .lib files for TSV models

This chapter is dedicated to a number of Computer Aided Design (CAD) tools developed throughout this thesis aiming to automate and speedup a lot of critical and time intensive parts of the 3D integration flow. The CAD tools developed aim to extend the current standard digital design flow of 2D into a 3D flow with the minimum involvement of the designer.

The procedure of .cir to .lib file creation has some complexity because of the many combinations that take part. Particularly, when we want to convert a .cir file to .lib file we should follow the following procedure. First we must choose the model's netlist described in a .cir file and then we must do a lot of combinations to generate the .lib file. This procedure is too difficult for someone to attempt manually. The aim of this report is to demonstrate a cad-tool developed to allow the automatic conversion of .cir files to .lib files in combination with automatic hspice simulation. One important advantage of this cad-tool is that it gives to the user the option to change the R-L-C element values of the .cir file through a Graphic User Interface (GUI). The cad-tool and its options will be presented more analytically below.

4.1 Theory and Analysis

The first idea was to create a cad-tool customized to the user needs. To reach this goal we considered that giving the user the freedom to choose his own TSV model to create the .lib file for his netlist will be very helpful. To make the tool even more functional, we consider that it is important to give an option to the user to change the TSV element values, for instance the R-L-C values, with values better matching his model.

The main concept to do this, is described below. Firstly, a user loads his own .cir file which describes the TSV model that he wants to use to create the library file. Then, through the GUI he is allowed to change the TSV element values. Then, his TSV model netlist is ready to use to export the corresponding .lib file.

A library file is used to synthesize an RTL Verilog/VHDL file to a netlist. A library file specifies what cells are in our library, their functions, pin names, timing/power characteristics. The library definition file is separated into two sections: a header section that defines attributes to be used by all cells in the library, and cell section that has a definition for each cell in the library. A cell's definition defines attributes about the cell such as pin names, area, functionality, timing, power, etc.

4.2 Algorithm for the .lib files creation

4.2.1. Flow

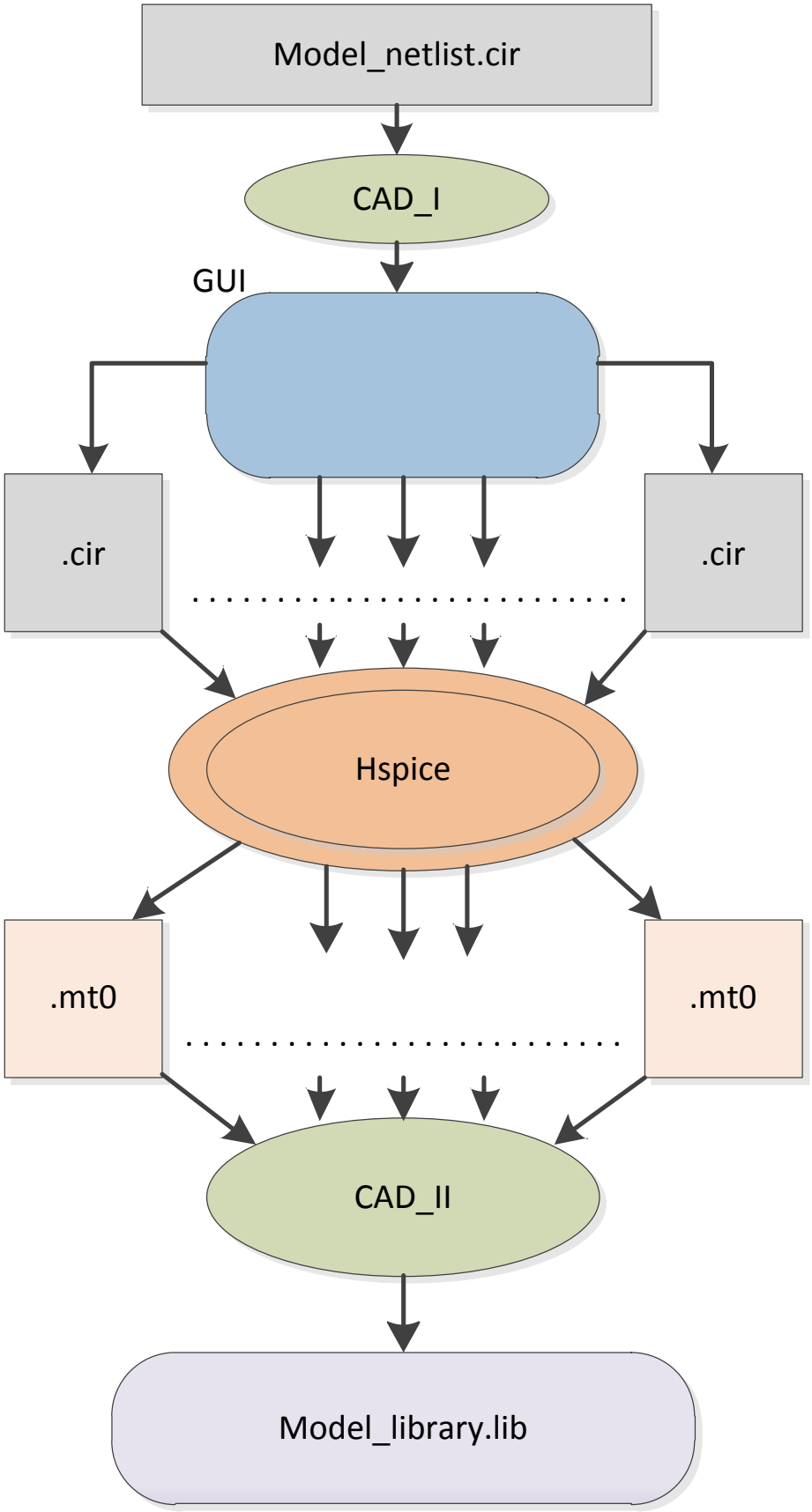


Figure 4-1 Flow diagram for the Cad-tool

Our .lib files will be used from Synopsys for timing analysis (Synopsys supports multiple timing models). The basic idea of our model is to define a voltage source input (Vsignal) for input and a capacitive load as output. The input net transition timing and the capacitive loads are used in order to create the library file. As Vsignal we use the "V_rise_trans" for the rise signal and the "V_fall_trans" for the fall signal with seven different values each other. To initialize the Vsignal we use the Piecewise linear source (PWL) with the drift for different times as arguments.

E.g. `V_rise_trans 10 0 PWL(0 0 0.1p 0 0.128p 1 5p 1)`

We can easily notice and also verify the rise and the fall signal from the graph that occurred from the arguments. Finally, the measures were taken at the 10 to 1 nodes. As a capacitive load we define a "C_trans" with seven different values as well (nodes 1 to 0).

For the transient analysis we use the following functions:

```
MEAS TRAN Tdelay TRIG V(10) VAL=0.5 RISE=1  + TARG V(1) VAL=0.5 RISE=1
With this command we calculate the delay at the first rise at the 0.5
point.

MEAS TRAN Tdelay TRIG V(10) VAL=0.5 FALL=1  + TARG V(1) VAL=0.5 RISE=1
Allows us to calculate the delay at the first fall and the first rise at
the 0.5 point.

MEAS TRAN Trise TRIG V(1) VAL=0.3 RISE=1 TARG V(1) VAL=0.7 RISE=1
We calculate accurately the rise time at the first rise  at  the 0.3 and
0.7 points.

MEAS TRAN Tfall TRIG V(1) VAL=0.7 FALL=1 TARG V(1) VAL=0.3 FALL=1
We calculate the fall time of the output signal at the first fall of the
input signal at the 0.3 and 0.7 points.
```

All these results taken from the hspice concluded to the "trans" folder with the suffix .mt0.

To sum up, to create a library file we need four functions, the cell_rise, rise_transition, cell_fall and fall_transition. The rise and the fall functions take as arguments two indexes. index1 and index2. Index1 has the transition times for the rise and the fall signal from every capacitive load, which are standard from the user. Index2 contains the capacitive load values. There is a 7x7 table named "values" as another argument, which contains the V_rise_trans-C_trans and V_fall_trans-C_trans

combinations. More specifically at the first row-first column there is a V_rise_trans-C_trans combination, at the second row-first column is the V_rise_trans'-C_trans combination. The V_rise_trans value changes by row and the C_trans by column. In this way we continue by filling all the tables.

4.2.2. Implementation

The first goal was to create a GUI in java that loads the .cir file for .lib file creation. With this GUI we give the user the choice to change the values of the R-L-C circuit elements to his needs. The user can execute the cad_tool by executing:

```
> path_of_java_installation/java TSVLibGeneratorCore
model_path/model_filename.cir
```

from the cad tool installation folder. The TSVLibGeneratorCore contains the main function of the project and the model_filename.cir is the .cir model the user wants to use to export the .lib file. Then a window appears with R-L-C cells in which we can fill the desired values.

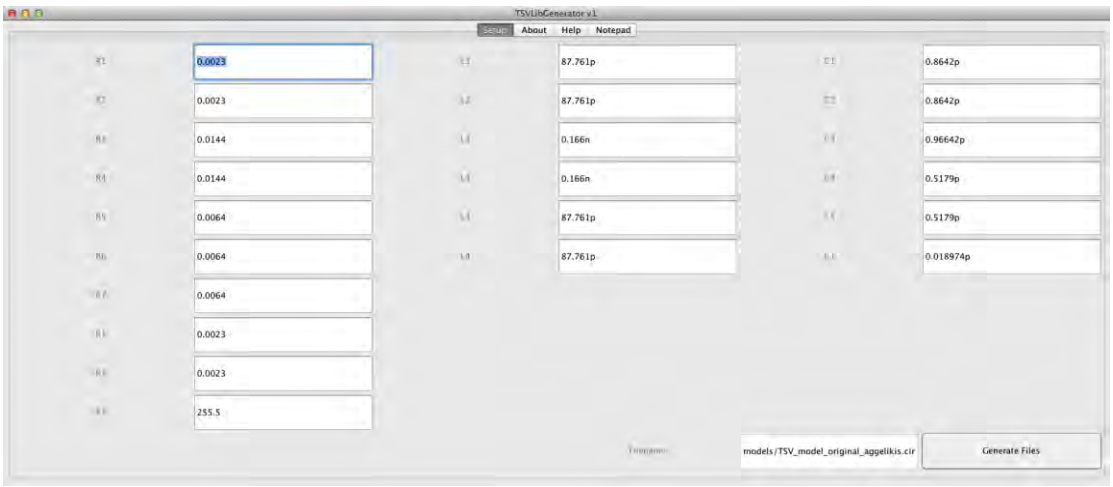


Figure 4-2 GUI allowing changing circuit's element values

The updated .cir files are then generated once the user presses the “Generate Files” button. You can found all the .cir files in the “trans” folder. The final state of this step is all the .cir files with all the V_rise/fall_trans-C_trans combinations generated.

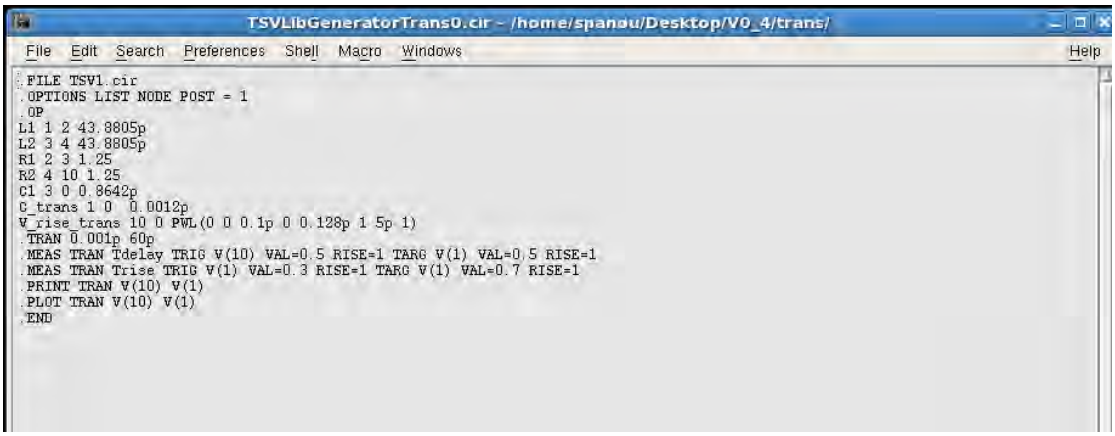


Figure 4-3 Example of generated .cir files for transient analysis

Later on, we must find the delay and fall-rise time for each .cir file. One way to do this step is manually. The vast number of values involved suggests the requirement to automatically convert all the .cir files to .mt0 files. The .mt0 files contain all the information about the delay and the fall-rise time we need. This procedure could be done with the use of hspice tool. Instead of performing each simulation by hand, a script was developed to perform all the simulations automatically.

The script can be executed by the following command:

```
folder_contains_script> ./hspiceTSVLibGenerator
```

where the hspiceTSVLibGenerator is our script.

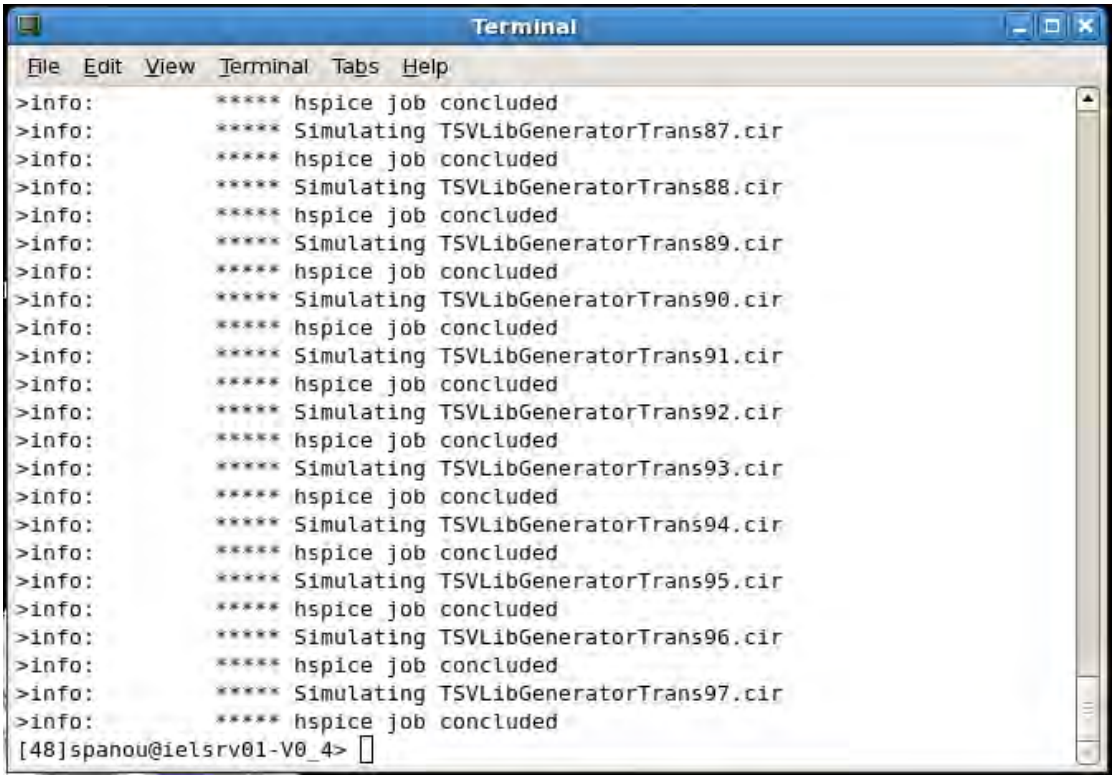


Figure 4-4 The .cir file simulation and .mt0 file creation

These step's result is all the .mt0 files be generated in the folder "trans" as foretold.

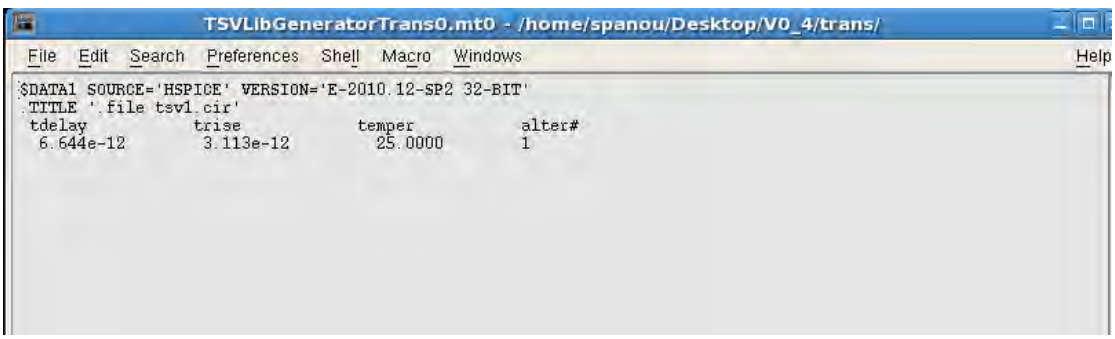


Figure 4-5 Contents of.mt0 file

The next step to reach the final goal, the library file generation, is to fill the .lib file with the information that we acquired from the previous step. For this reason a second cad_tool

(TSVLibExtractor) has been developed. Via this cad_tool all the delay and fall-rise time values are inserted and sorted to the tables of the .lib file as mentioned before.

To execute the TSVLibExtractor cad_tool:

```
path_of_java_installation/java TSVLibExtractorCore library_filename.lib
```

Similarily to the TSVLibGenerator, “TSVLibExtractorCore” contains the main function that generates from the .mt0 files generated earlier the library_filename.lib file the user requires.

The library_filename.lib file is created inside the folder “lib”.

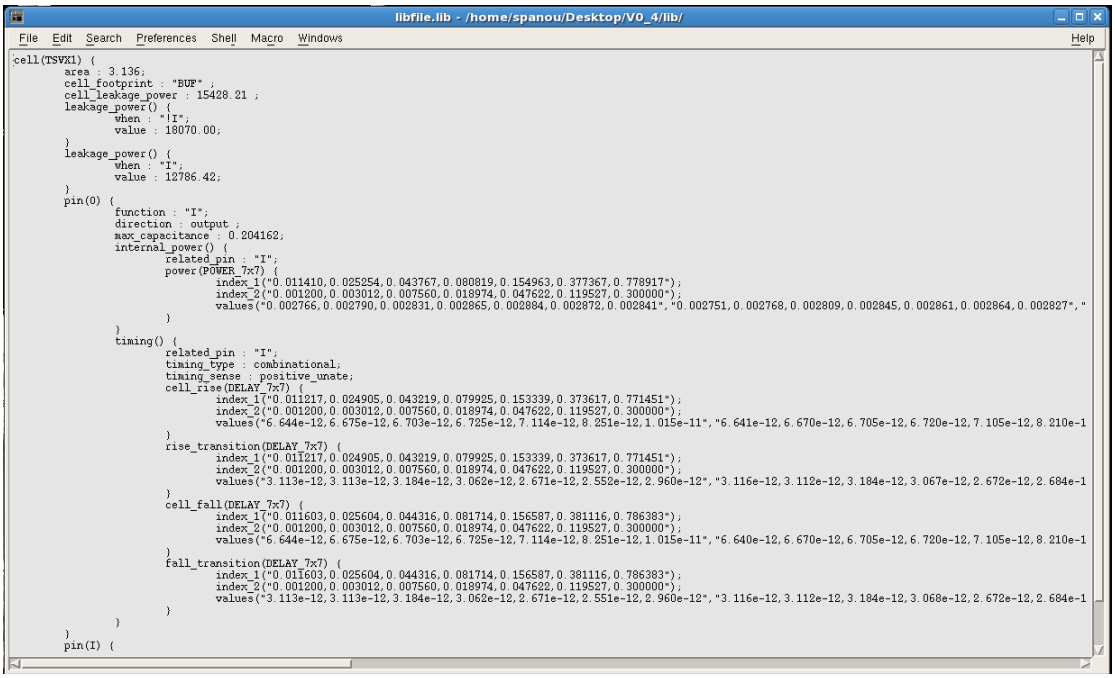


Figure 4-6 Contents of .lib file generated

The next step will be the .lib(*1) to .db(*2) file conversion, because before a library can be used, it must be compiled.

The dc_shell program is a command line interface to Synopsys Design Compiler. To compile a .lib file to .db format, we execute:

```
% dc_shell
dc_shell > read_lib sc_cadence.lib
dc_shell > write_lib sc_cadence
dc_shell > quit
%
```

*1. The ASCII form of the library is usually has a '.lib' extension

*2. The .db format is a binary format used by Synopsys for compiled designs/libraries

4.3 Example Model

In this chapter some models for library file creation are presented. We must underline that, the input and output for the measurements are considered the nodes 10 (as input node) and 1 (as output node). As a result, the user must customize his netlist to this model.

Model:

```
// single TSV (Ctsv connected to gnd)
.FILE TSV1.cir
.OPTIONS LIST NODE POST = 1
.OP
L1  1   2  43.8805p
L2  3   4  43.8805p
R1  2   3  1.25
R2  4   10  1.25
C1  3   0  0.8642p
.END
```

4.4 TSVPort Redirect

In this section a cad tool aiming to speedup and ease the integration of our flow to the standard flow by automatically distributing 2D designs to 3D is presented. This cad tool, namely TSVPortRedirect, aims to ease the process of distributing the design into 3D by automatically altering VHDL files to redirect 2D signals to TSV transmitters or receivers thus converting them to 3D signals. The choice of signals to be redirected still relies on the designer but from that point on the process is automated. The concept of the tool is that the designer specifies the signals he wants to pass to or receive from a different 3D layer and also provides the original VHDL of his (2D) design. The tool then automatically generates the VHDL code including the transmitters and the receivers as components in the VHDL and redirects the corresponding signals, specified by the designer, to them. The transmitter and receivers that are inserted as components in the VHDL were created and are included in the package and are presented in detail in the next chapter.

Syntax:

```
TSVPortRedirect <VHDL_input_file> <VHDL_output_file>-
tx(list_of_signals_to_be_transmitted) -rx(list_of_signals_to_be_received)
```

Arguments:

VHDL_input_file:	filename of the VHDL file to be converted. (Compulsory)
VHDL_output_file:	filename of the VHDL file to be generated. (Compulsory)
list_of_signals_to_be_transmitted:	list of signals to be transmitted through TSVs, separated by comas. (Optional)
list_of_signals_to_be_received:	list of signals to be received through TSVs, separated by comas. (Optional)

To conclude, in this chapter a flow and a number of cad tools, which automatically convert .cir files to .lib files with the combination of automatic hspice simulations, were demonstrated. The most important goal reached is the automation of the library file creation procedure. However, the key feature of these cad tools is the customization to the user needs. With these cad tools we achieved

the automation of the procedure, saving time for the user, avoiding manual involvement (thus reducing the possibility of errors) and hiding the significant complexity of the process.

Chapter 5. Physical layout

In this chapter the procedure of physical layout of a TSV model will be described. In the previous chapters we mentioned the first steps, create a TSV model, analyze timing parameters, convert .cir files to .lib files and use them to the Design compiler to conclude with the final step, the final circuit creation. Specifically this chapter concentrates on creating a final product and it describes step by step this process. Firstly, we will talk about the schematic of the TSV model we choose to create and then we will refer how we take the final physical layout from the schematic.

5.1 The model

We use a schematic model of a low-swing TX transmitter and a gate-diode sense amplifier-based RX as a receiver in order to create a compact low-power 3-D I/O in 65nm CMOS.

With potentially thousands of multi-Gb/s I/O, support for tens of Tb/s data bandwidth between the local chip can be activated by the 3D integration technology, but this ultra high bandwidth will be achieved only if the area meet the challenges on the energy performance of 3D I/O.

Because 3D interface offers reduced load and therefore improved signal integrity compared to traditional channels between the chip, 3D chip I/O does not require complex, power-hungry balancing regimes.

Reduced swing approaches offer a path to further Power reduction for 3D I / O, but the receivers for low-swing schemes are usually complex and consume large area and power and this is what we want to solve with the lower-power 3-D cross chip I/O.

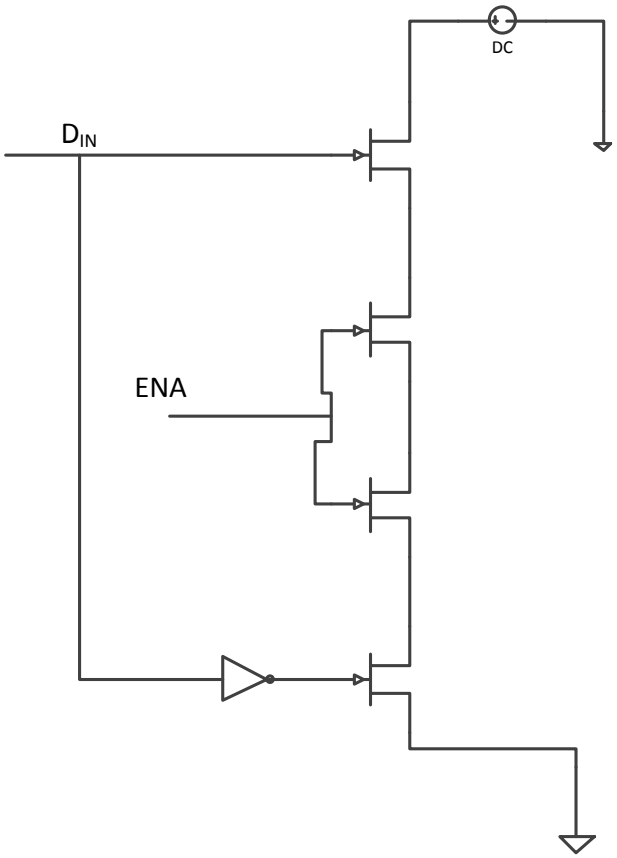


Figure 5-1 The transmitter

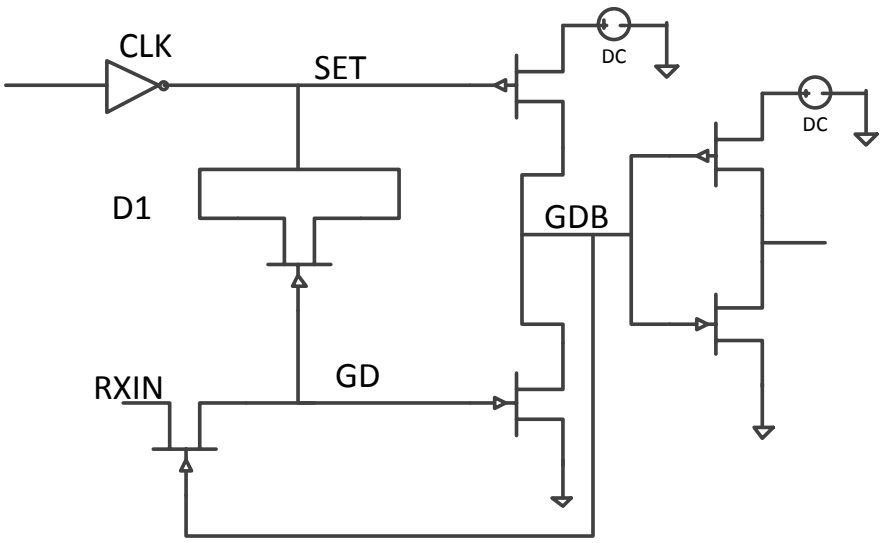


Figure 5-2 The receiver

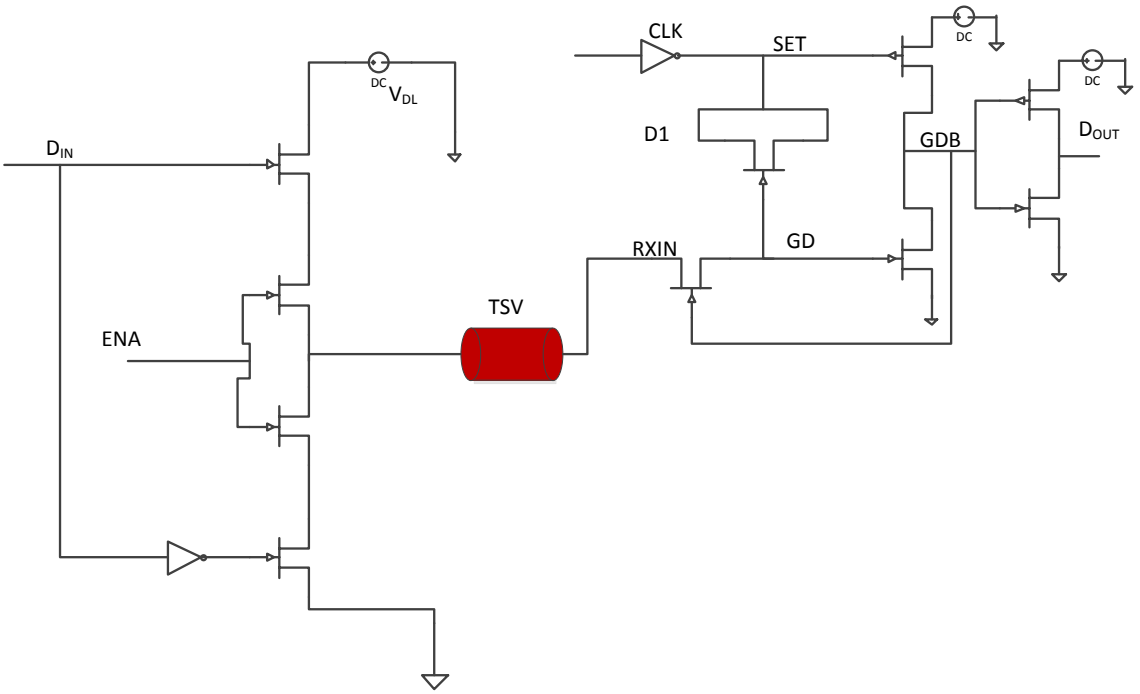


Figure 5-3 The final circuit with a TSV

5.2 The schematic process

In this section we will design our own schematic. Then we will determine transistor sizes and, with the insight provided by simulation results, verify and optimize the design.

Firstly, we open the Cadence and we design all the sub-circuits, the transmitter (TX), the receiver (RX), the single TSV model and the inverter. More specifically, we should use either Add→ Instance from the menu or press “i” to add a circuit component and Add→ Pin or press “p” to add pins to the schematic. The supplies VDD and VSS are set as input/output.

The bulk of the N-MOS transistors should be connected to the lowest possible voltage level (VSS) and the bulk of the P-MOS transistors should be connected to the highest possible voltage level (VDD).

Finally, we use the Add→ Wire (narrow) or press “w” from the menu to add connections to our schematic in order to connect the different elements.

To make our design more compatible with the new designs that offer less power and good characteristics, we gave special attention to transistor model and sizing. We observed the behavior of the circuit from the plot waves and changed the transistor values unless we noticed a pulse that is nearest to our ideal model pulse.

So, we reached to the followings:

For the transmitter we use SPHVT (high voltage threshold) transistors with values for n-MOS transistors:

Length=60nm

w=10um

and VDL=300mV (low voltage)

For the receiver we use PSPLVT (p-MOS-low voltage threshold) and NSPVLT (n-MOS-low voltage threshold) transistors with values:

For n-MOS

Length = 60nm

W = 4um

But for the NM9

Length =60nm

w=6um

Later on we change the inverter values as well to help the circuit works properly.

We resulted to the following values.

Length =60nm

w=2um

for n and p transistors.

When the operation is completed, we proceed by choosing “Check and Save” your schematic to correct any errors or warnings until none is any more reported.

The next step was to create a new symbol for all the components we design to connect them all together to create the finally circuit.

Finally we set the Din with period 4ns and the CLK with period 800ps.

The next step was to simulating the performance of our design to understand if it works properly.We open the simulation environment by clicking on Tools→ Analog Environment on the very left upper corner of the schematic window. Analog Design Environment window will pop-up as shown in Fig. 5-4.

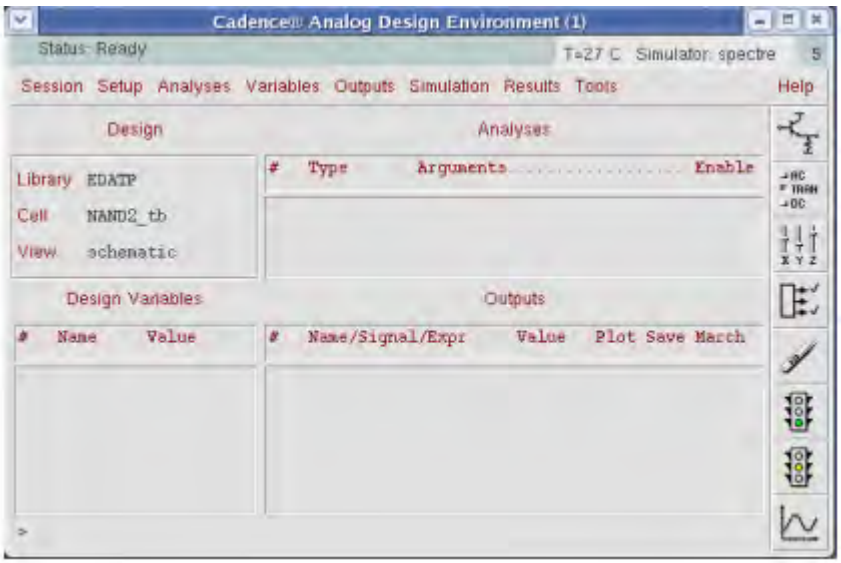


Figure 5-4 Cadence Analog Design Enviroment

We use Analysis→ Choose in order to select the type of simulation you would like to run.

In the pop-up window, edit the necessary properties as shown in Fig. 5-5.

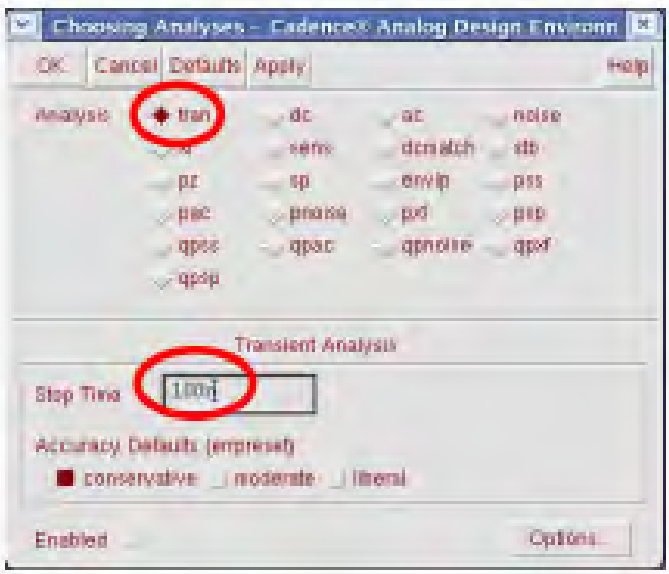


Figure 5-5 Checking transient analysis

We set the Analysis type to tran (transient) with 10ns stop time.

We use Outputs→ To be Plotted→ Select on Schematic command in the Analog Design Environment to displayed the point we want from our schematic to a plot.

To run a simulation, we use Simulation→ Netlist and "Run" command from the Analog Design Environment window and if we are not have errors the plot window appears.

In our case we take the following plots:

Figure 5-6 The results from the transient analysis

To split the Waveform window view into multiple graphs, we use Axes→ To Strip command.

We notice that the results are very close to the ideal results, so we can go on with the physical layout.

5.3 Physical Layout

Finally, after the design has been validated, we will create the mask layout of this component and check the design rules for it.

Generally, we must design the transmitter and the receiver in a physical layout, with metals and rules that depends on the technology we use. In our case we use the 65nm technology so we design the components with these rules.

This process was done with the help of cadence virtuoso editor which is a tool used as a layout editor. So, the goal of this session will be to draw a layout for the transmitter (TX) and the receiver (RX) and check it for Design Rules.

The first step was to create a new cell view in our new library. We select our library and TX cell and RX cell each time and we choose File→ New→ CellView.

We Select layout as the view name.

But at the Tool field it should be written “Viruoso” as a layout editor.

All available layers and their related design rules are provided in the 0.65um technology Design. Minimum spacing between various layers and minimum width specification of all layers are the most critical rules to be respected.

The most important layers we used are NTUB, DIFF, POLY1, PPLUS, NPLUS, CONT and MET1.

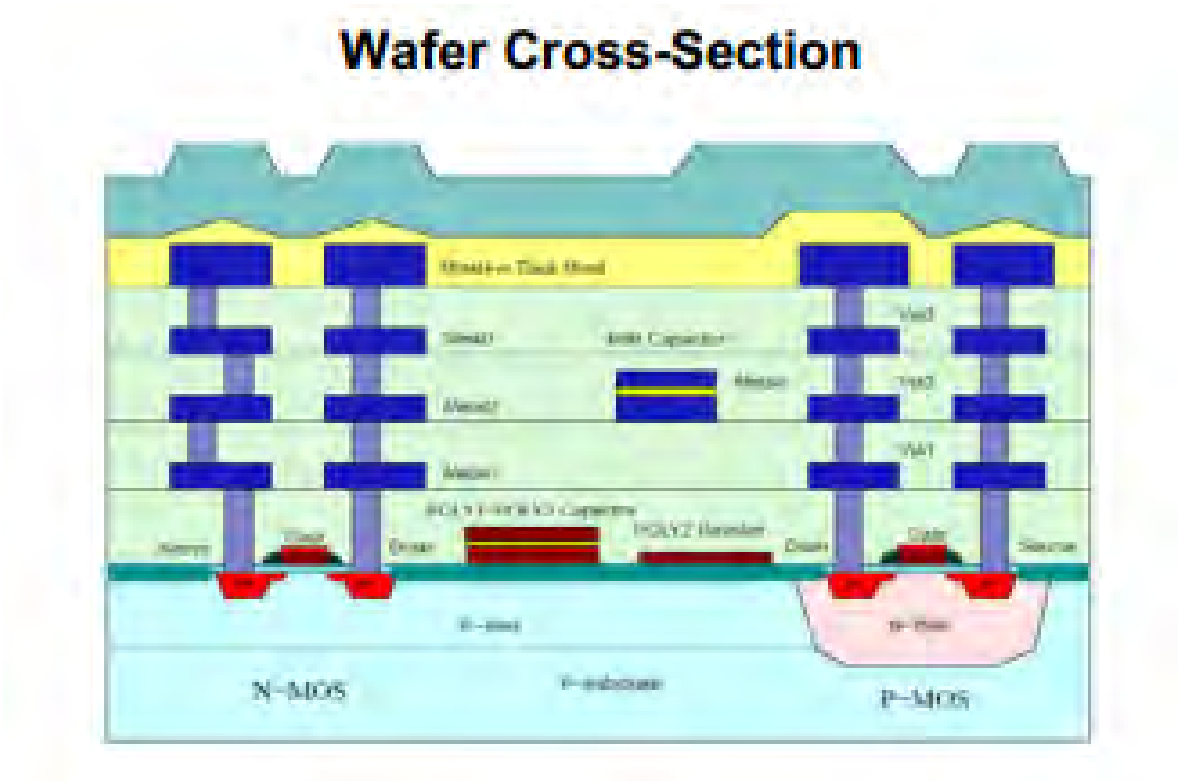


Figure 5-7 Cross section and layout of a MOS transistor

The initial Virtuoso Layout Editor window in which you will draw your layout and the LSW-Layer Selection Window are displayed in Fig. 5-8.

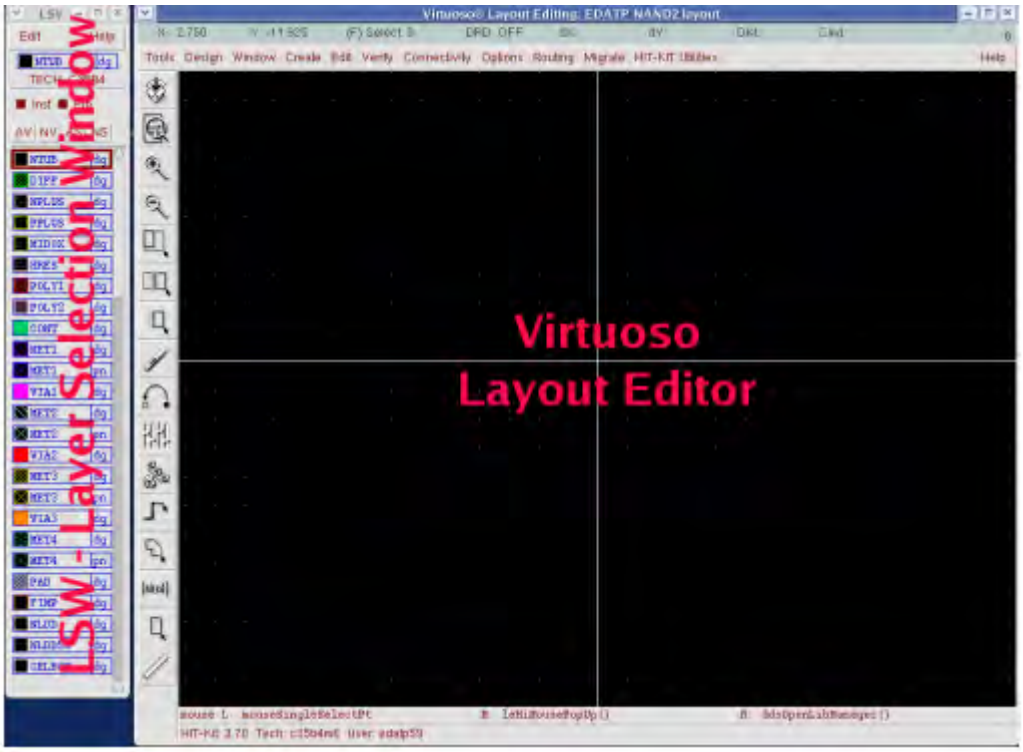


Figure 5-8 Initial layout Editor window

Each layer in the LSW consists of a layer texture, a layer name and a layer type (Fig. 5-9 is an example for POLY1 dg layer). We should always use drawing - dg layer type (not pn) unless it is explicitly said to do differently.

Left click on a layer in the LSW for selecting that layer (marked with red frame in Fig. 5-9).You can then use it for drawing.

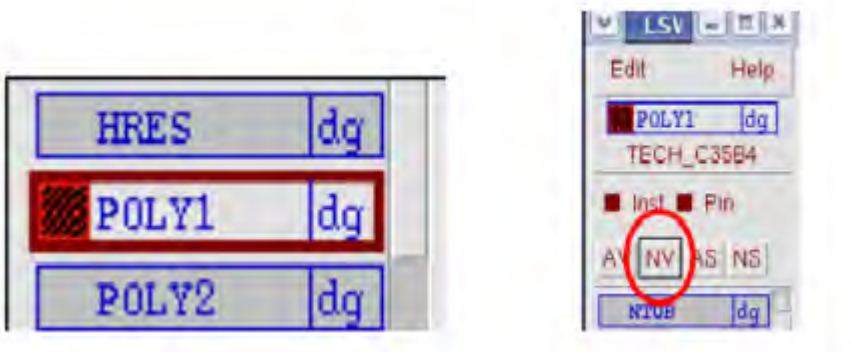


Figure 5-9 The LSW in detail

The basic metals that we use were the MET1 for the transistors source and drain and the POLY1 for the gate.

The final layout for the transmitter and receiver can be seen in Fig. 5-10 – 5-11 below and the final 3D I/O chip stack can be seen in Fig. 5-16.

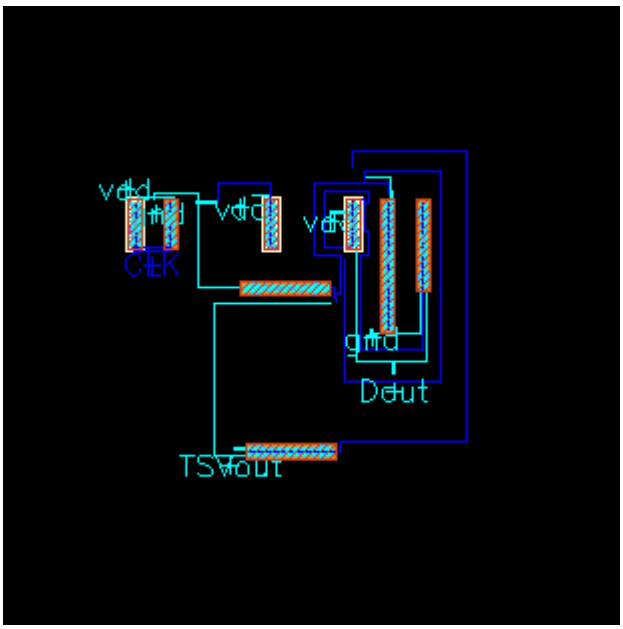


Figure 5-10 The layout of the receiver

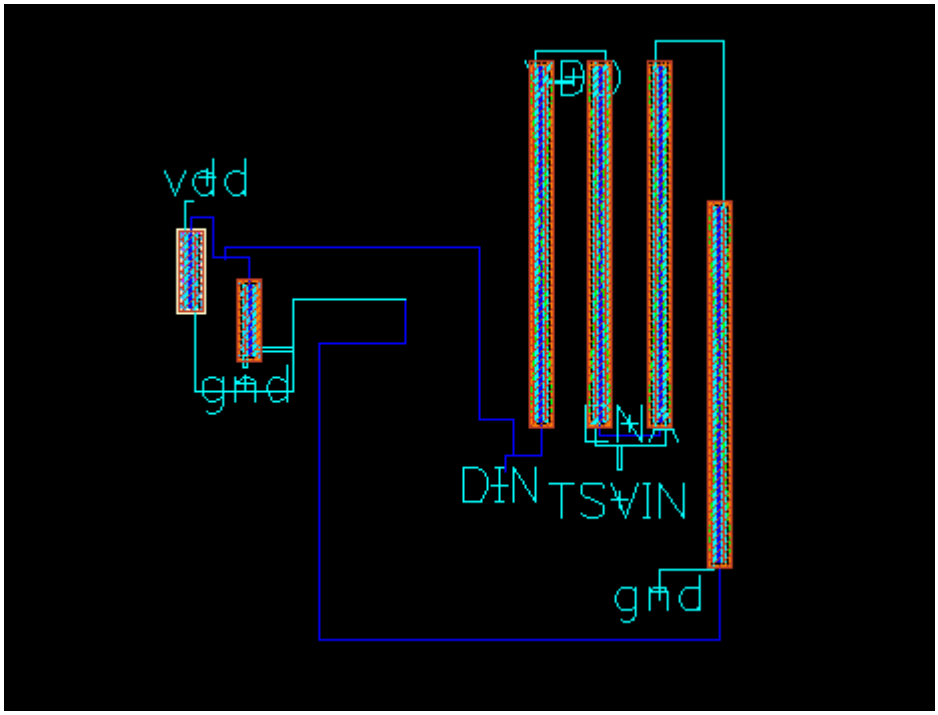


Figure 5-11 The layout of the transmitter

When we draw a transistor in physical layout we should understand its structure and how impress it to a wafer. A wafer consists of silicon (Si). At the first level we put the implant that depends on the transistor type. For n-MOS transistor a N-well (NTUB) is needed extra. The second level consists of diffusion and the third level from MET1 for metal connection. To contact the MET1 with the silicon, we use contact cuts (CONT). For the gate we use the Polysilicon Gate (POLY1).

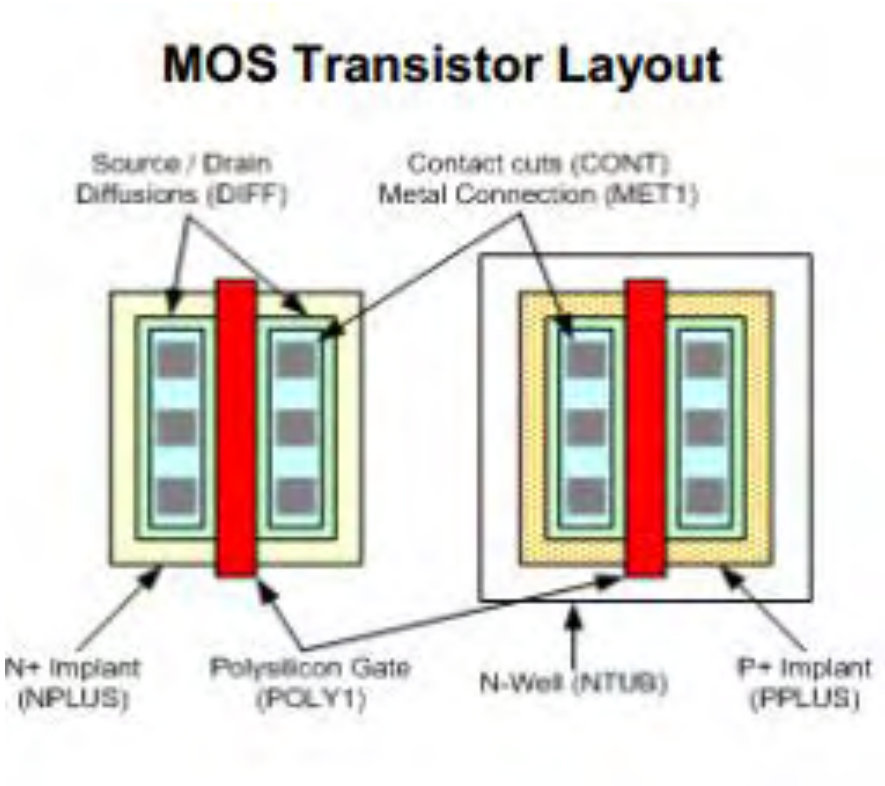


Figure 5-12 Layout of a MOS transistor

After having drawn the layout, it is necessary we do a Design Rules Check (DRC). We did a Design→ Save(or press “F2”).

We use Assura→ Run DRC from Layout Editor menu to start the DRC dialog and we click on Set Switches field and perform the selection according to Fig. 5-13.

Then we click on OK to run the DRC.

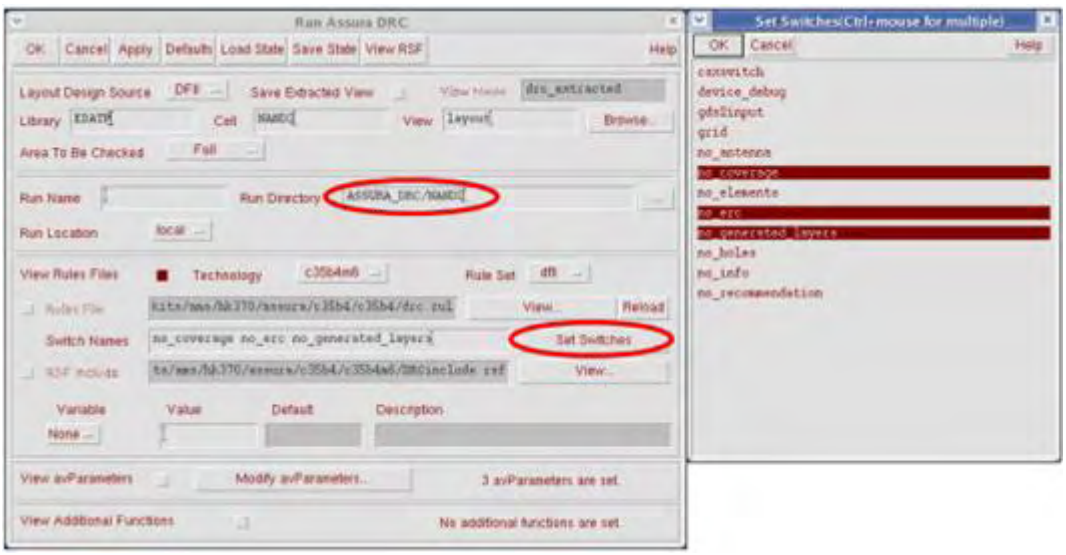


Figure 5-13 The Assura set up

In case the DRC has detected some errors, the Error Layer Window will pop-up.

We repeat DRC procedure until we got the message “No DRC errors found” after we corrected all the errors.

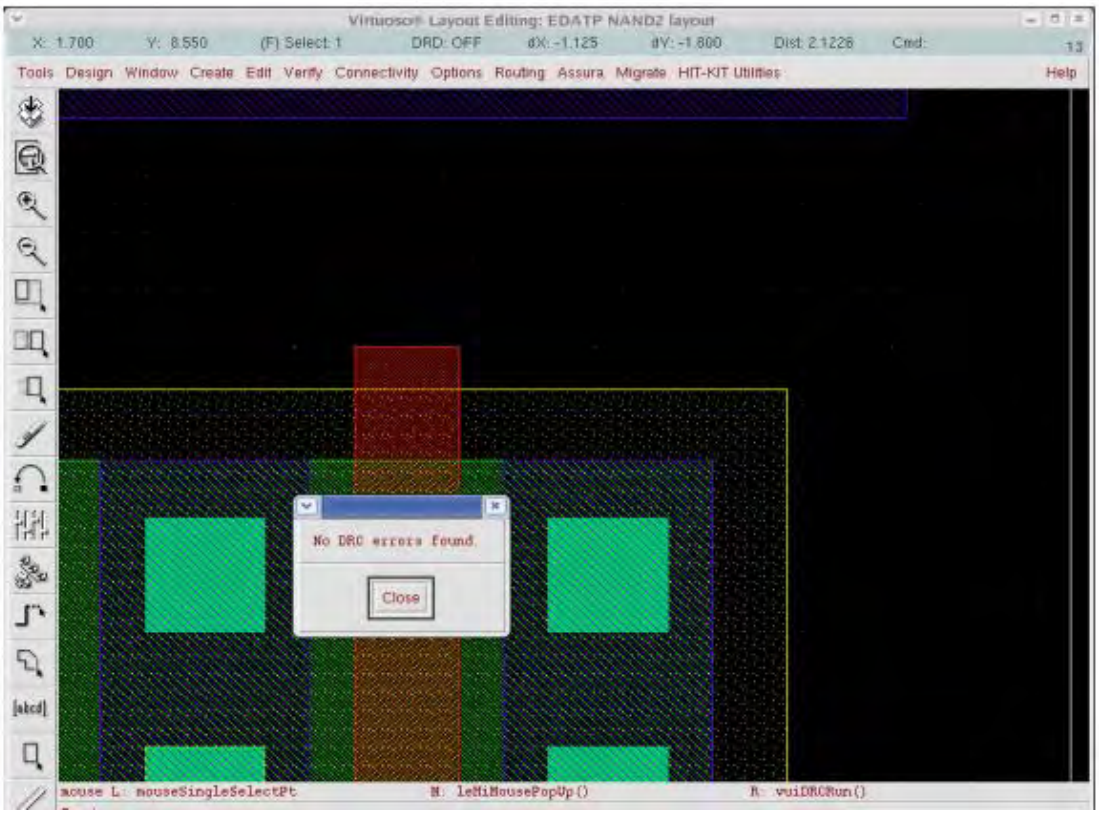


Figure 5-14 Clean DRC, no errors.

In some cases it is important to do a LVS rule check that checks if the layout we design has the same connections with the previous schematic.

We use Assura→ Run LVS from Layout Editor menu to start the LVS dialog and we click on Set Switches field and perform the selection according to Fig. 5-15 .

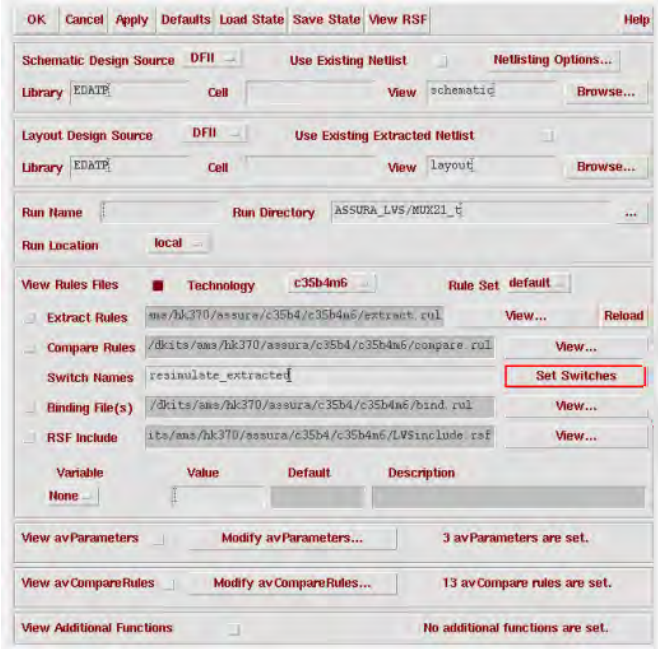


Figure 5-15 LVS Setup

Then we click on OK to run the LVS.

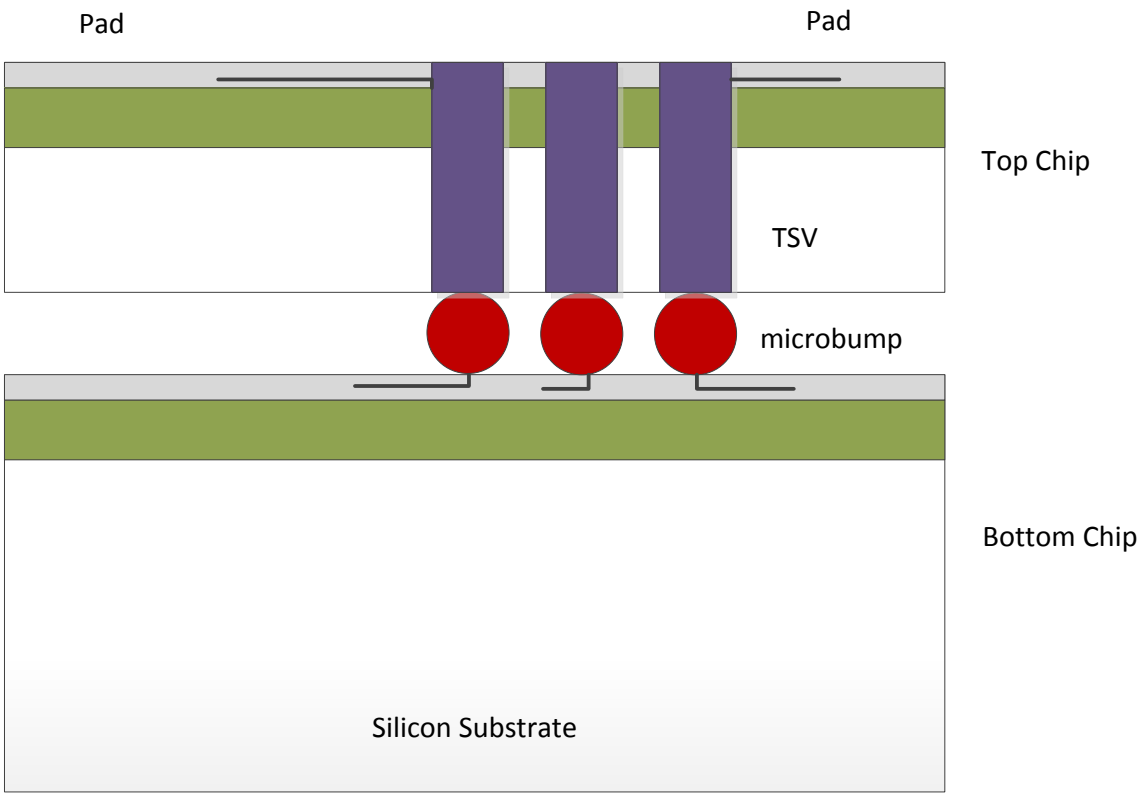


Figure 5-16 3D I/O chip stack

Chapter 6. Conclusion

This thesis demonstrated the attempt to validate and refine EPFL's 3D integration technology. It additionally proposed a novel 3D design flow by extending the standard 2D digital design flow. The whole process was speed up and its complexity was reduced by a set of CAD tools.

TSVs were modeled physically concerning resistance, inductance, and capacitance in order to determine their impact on the performance. Overall, five different models were introduced and discussed.

In order to model the TSVs accurately, radiofrequency measurements were performed and included in detail. The measurement procedure, as well as, the equipment used was discussed. The values of the MOS-capacitor extracted by theoretical mathematic models were also compared to the experimental measurements. This value of MOS-capacitor can be the beginning for TSV model expansion in the future.

A number of CAD tools that extend the current standard digital design flow of 2D into a 3D flow and aim to automate and speedup the most critical and time intensive parts of the 3D integration flow were developed and discussed. They were designed to require the minimum involvement of the designer.

The procedure of physical layout of a TSV transmitter and receiver to be used in par with the TSV models developed earlier was also described in detail.

Overall, starting with the creation of a TSV model, then analyze its timing parameters, include them in .cir files that are then automatically converted to .lib files through our CAD tools and then used in Synopsys Design Compiler we manage to arrive to a final product.

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APPENDIXES

Appendix A

A.1 RF measurements in 3 frequencies

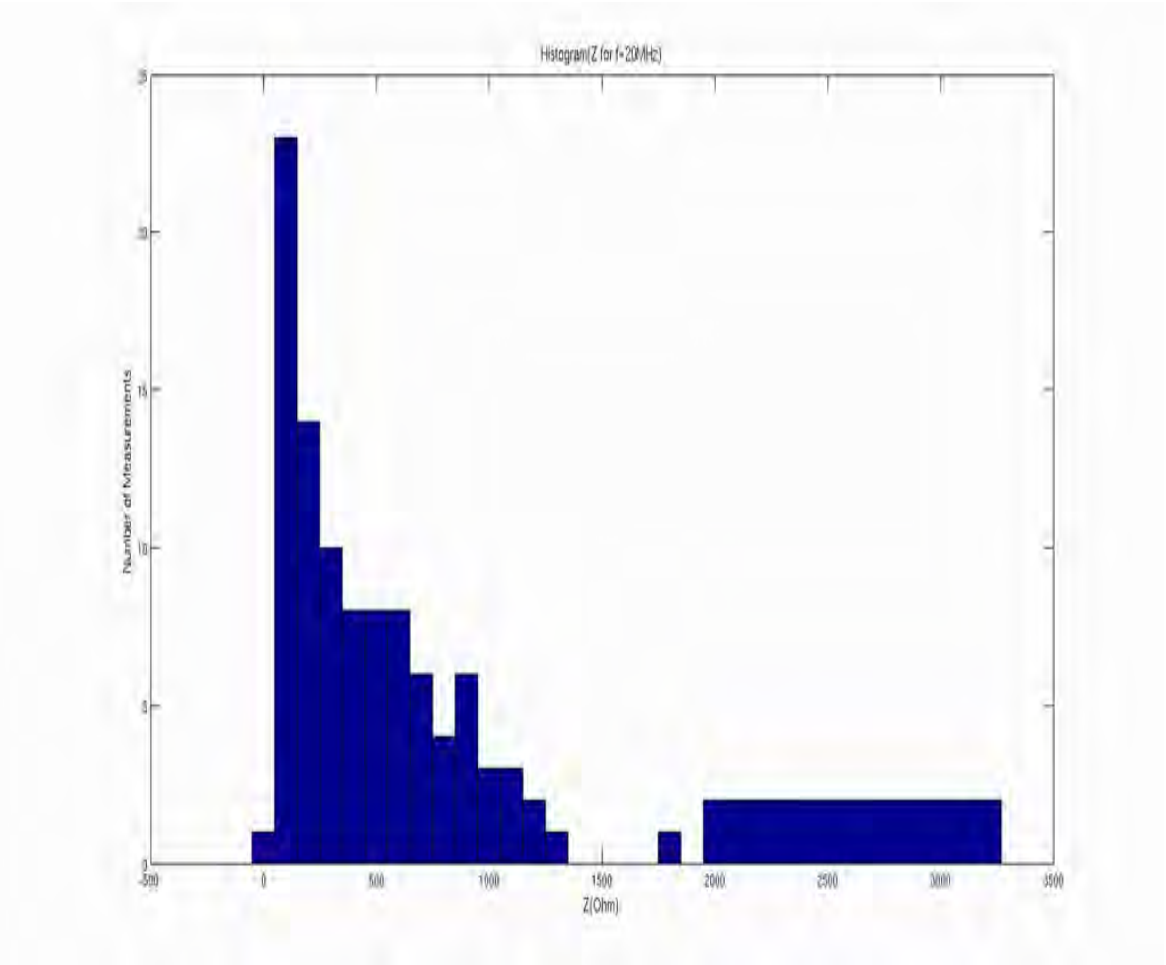
Impedance

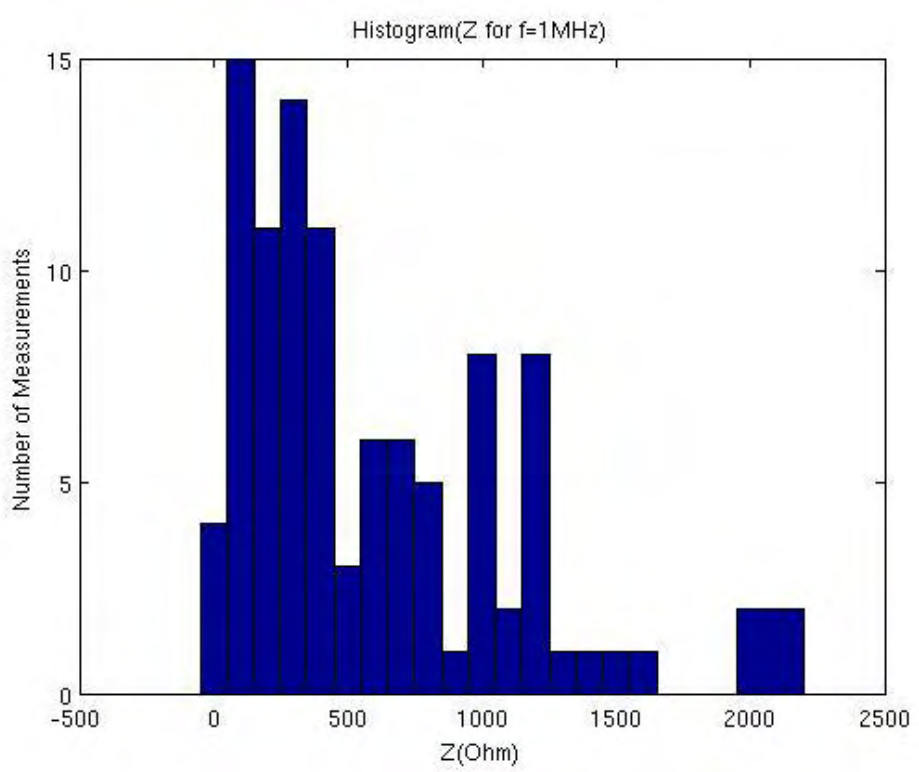
No. of measurement	f = 1 MHz	f = 10 MHz	f = 20 MHz
1	1.02*10^3	1*10^3	811
2	2.2	73	92
3	1.24*10^3	1.16*10^3	1*10^3
4	171	164	152
5	268	261	247
6	375	360	268
7	1.19*10^3	1.05*10^3	890
8	1.21*10^3	1.18*10^3	1.12*10^3
9	976	798	603
10	120	119	127
11	1.17*10^3	1.12*10^3	1.04*10^3
12	1.03*10^3	875	674
13	872	840	766
14	1.19*10^3	1.16*10^3	1.1*10^3
15	360	350	345
16	637	587	493
17	459	434	380
18	621	608	581
19	85	86	98
20	373	352	315
21	422	403	374
22	54	60	82
23	424	390	610
24	156	131	136
25	173	165	166
26	154	163	316
27	121	110	119
28	195	59	86
29	165	159	160
30	450	390	431
31	415	560	495
32	800	700	850
33	1*10^3	1.2*10^3	1.2
34	780	705	750
35	518	503	482
36	1.6*10^3	680	860

37	1*10^3	1*10^3	1.2*10^3
38	250	72	119
39	700	705	670
40	350	224	278
41	700	550	740
42	421	600	500
43	1.3*10^3	1.6*10^3	2*10^3
44	330	140	300
45	560	625	630
46	657	600	485
47	1.15*10^3	1.12*10^3	1.05*10^3
48	320	306	283
49	487	470	443
50	1*10^3	893	599
51	100	100	109
52	57	72	110
53	75	238	106
54	93	104	119
55	760	760	800
56	561	513	423
57	340	312	286
58	1.2*10^3	1.13*10^3	1.06*10^3
59	558	526	447
60	400	700	670
61	600	550	490
62	800	805	880
63	425	395	327
64	265	257	245
65	279	265	235
66	120	127	132
67	58	64	85
68	278	264	234
69	257	241	211
70	330	108	106
71	45	90	126
72	239	226	205
73	206	197	178
74	250	440	500
75	239	228	210
76	1.18*10^3	910	600
77	1.13*10^3	905	592
78	1.17*10^3	780	521
79	340	308	247
80	1.4*10^3	1.2	1.3
81	327	308	278
82	2*10^3	1.8*10^3	1.8*10^3
83	72	60	82
84	426	400	358
85	92	100	117

86	700	350	404
87	42	49	74
88	48	55	79
89	150	156	164
90	750	700	580
91	740	702	680
92	1.5*10^3	1.3*10^3	950
93	260	300	250
94	1*10^3	988	910
95	810	540	337
96	140	139	147
97	140	150	136
98	33	42	71
99	258	242	22
100	1*10^3	996	860

Histograms for Impedance





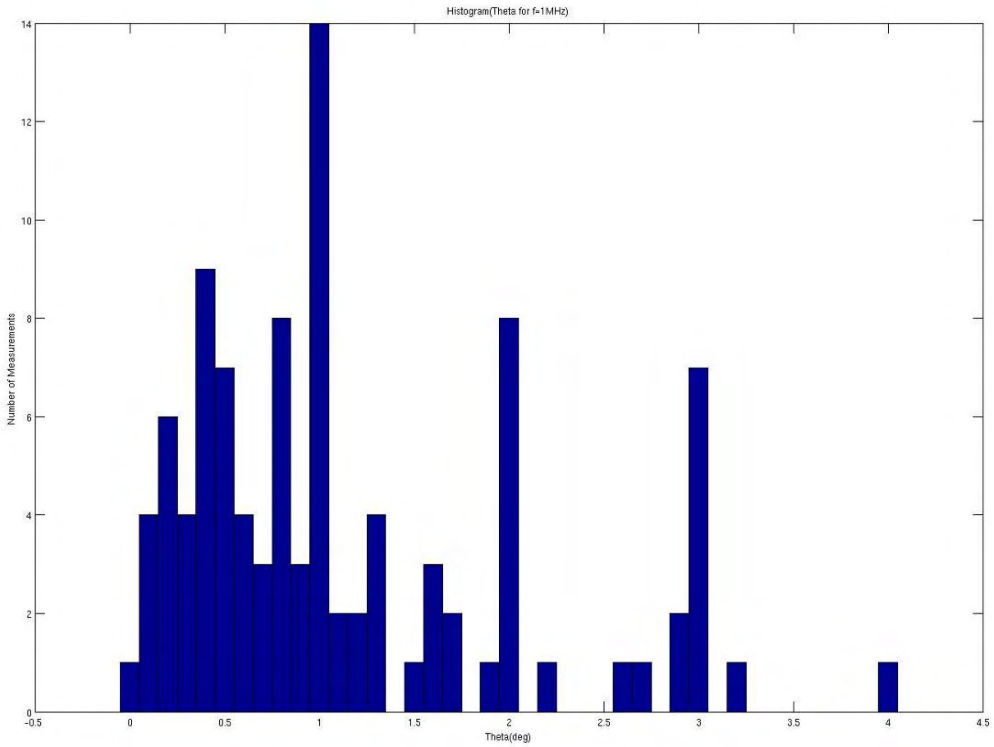
Theta

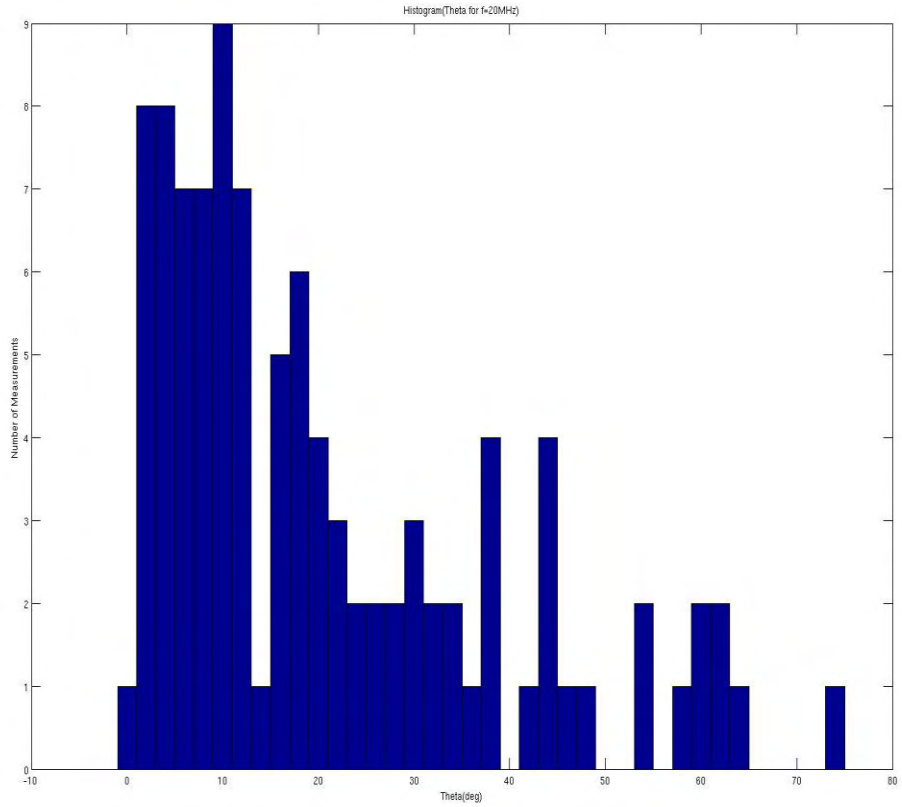
No. of measurement	f = 1 MHz	f = 10 MHz	f = 20 MHz
1	0.8	4.6	9.6
2	2.2	27	54
3	1.7	10	17
4	0.01	6.4	18
5	0.13	4.6	12
6	0.8	0.5	3
7	2.6	15	21
8	1.1	5	8.6
9	3.2	19	22
10	0.9	16	38
11	1.2	6.6	8
12	2.9	18	22
13	1.17	5	5
14	1.3	5.1	7
15	0.4	3.1	11.7
16	1.3	6.2	4.1
17	0.8	2.2	0.3
18	0.5	0.3	2.4
19	1.5	21	45
20	0.7	0.2	4.6

21	0.4	1.8	4.9
22	2.9	32	62
23	0.3	3.6	7
24	0.76	14	30
25	0.5	11	25
26	0.7	11	7
27	1	16	35
28	1	33	60
29	0.8	11.9	26
30	0.1	3.4	6
31	0.4	10	19
32	1	7	12
33	2	16	24
34	1	5	11
35	0.4	1.5	2.7
36	2	14	30
37	2	10	19
38	1	32	54
39	0.6	10	19
40	0.8	11	22
41	2	12	21
42	0.5	9	17
43	1	10	27
44	0.5	10	20
45	0.3	8	18
46	1.3	8	13
47	0.1	0.7	2.4
48	0.4	2	7
49	0.5	1	3
50	3	22	35
51	1	17	39
52	1	27	45
53	1	10	49
54	1	22	46
55	0.2	8	17
56	1.6	8	12
57	0.5	1	2.6
58	0.9	3	9
59	0.9	4	8
60	0.7	7	11
61	0.8	3	6
62	0.4	2	11
63	1	6	9.5
64	0.1	4.4	11
65	0.6	0.2	4
66	2	21	37
67	2.7	30	58
68	0.6	0.2	4
69	0.6	0.1	3

70	0.2	7	8
71	3	22	42
72	0.4	2	10
73	0.2	3	12
74	0.2	9	13
75	0.4	3	10
76	3	26	38
77	3	27	39
78	2	5	9
79	1	5	5
80	1	10	15
81	0.5	1	5
82	2	10	18
83	2	33	62
84	0.3	0.6	2
85	1.7	22	44
86	0.3	10	21
87	3	37	65
88	3	34	61
89	1	15	33
90	0.2	2.6	8
91	1.3	4	6
92	3	13	30
93	0.2	13	28
94	0.8	6	17
95	1.9	20	29
96	1.1	15	33
97	1.6	21	44
98	4	45	75
99	0.4	3	10
100	1.6	9	16

Histograms for Theta



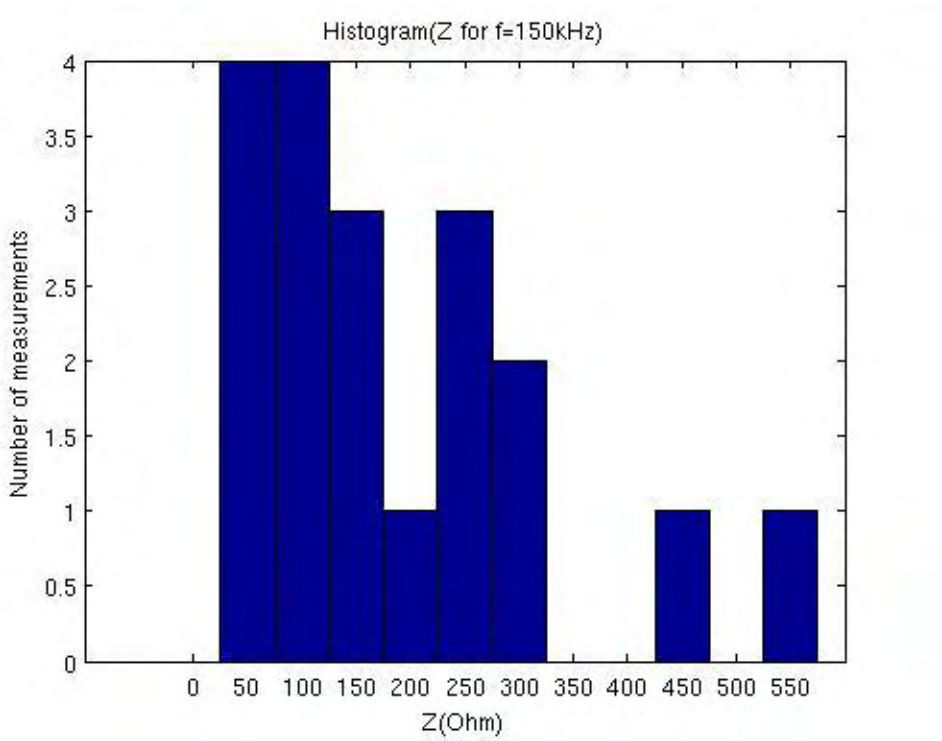


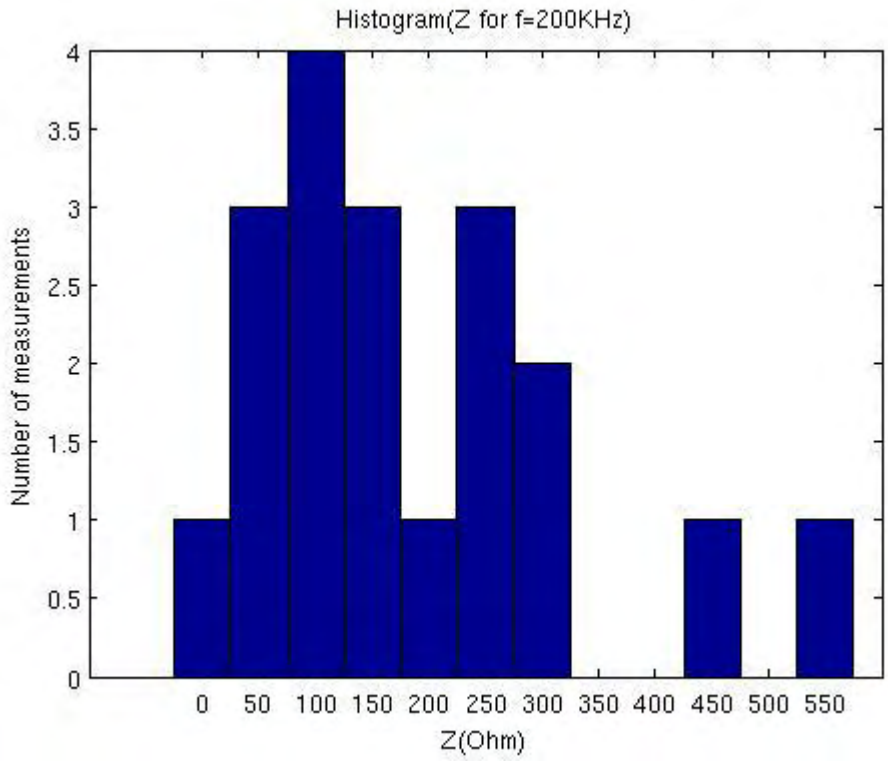
A.2 RF measurements in 20 frequencies

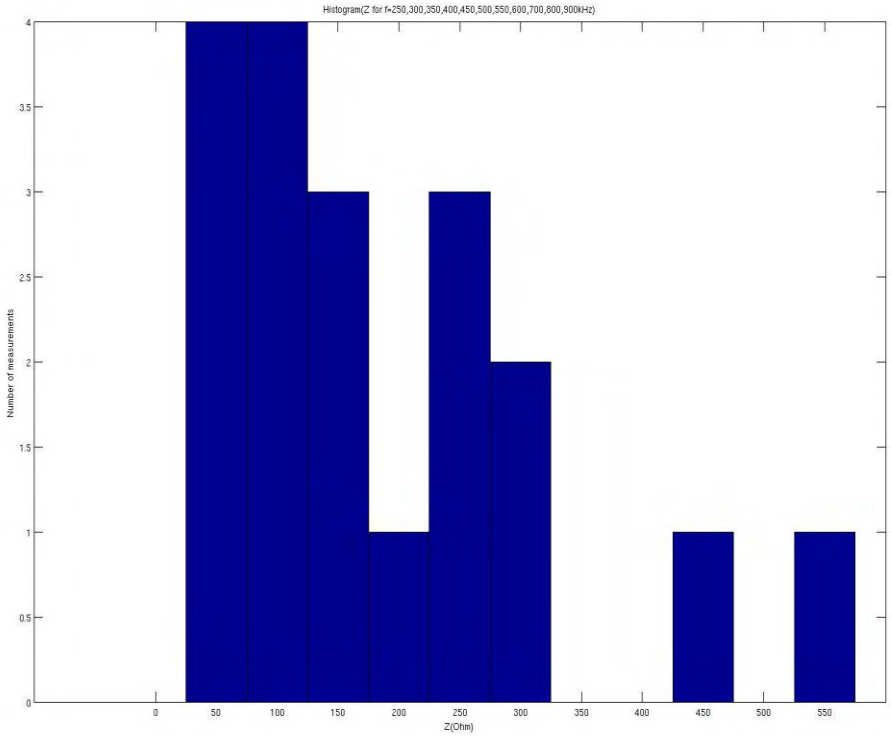
For Impedance

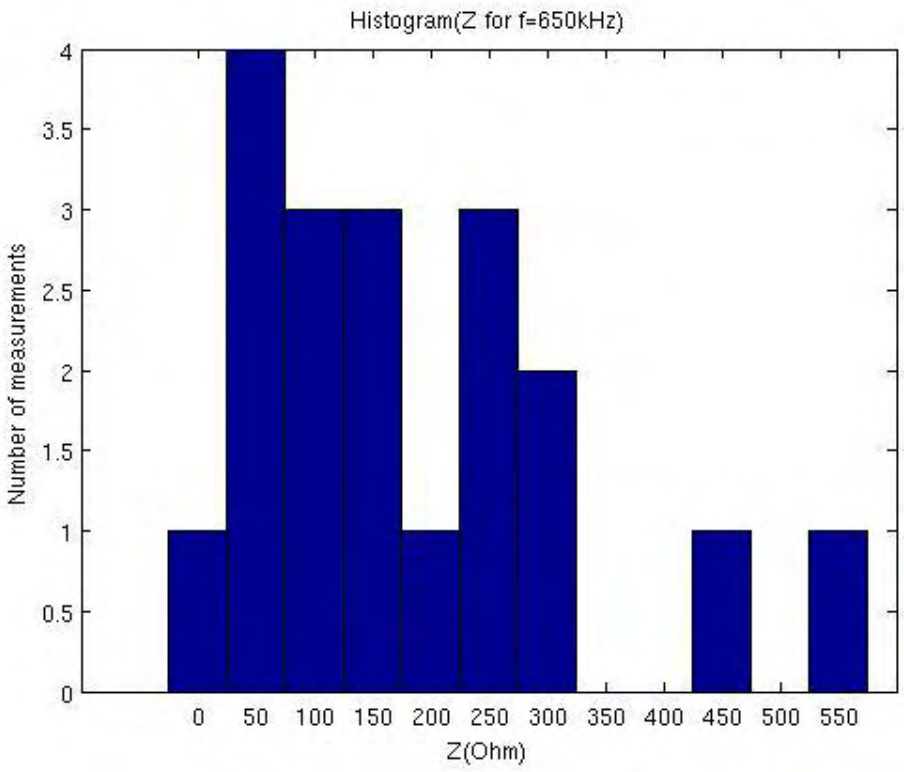
Fr /#	100 KHz	150 KHz	200 KHz	250 KHz	300 KHz	350 KHz	400 KHz	450 KHz	500 KHz	550 KHz	600 KHz	650 KHz	700 KHz	800 KHz	900 KHz	1 MHz	10 MHz	15 MHz	20 MHz	30 MHz
1	310	310	310	310	310	310	310	310	310	310	310	310	310	309	308	310	315	280	267	203
2	280	280	280	280	280	280	280	280	280	280	280	280	279	280	280	279	287	252	240	181
3	556	555	556	555	554	554	553	551	552	552	551	548	549	551	552	552	565	522	526	386
4	36	35	35.7	35	36	36	36	36	36	36.1	36	36	36	35.8	35.8	35.6	69	29	29	7
5	162	159	158	158	158	158	157	157	157	157	154	153	152	152	153	156	183	147	146	104
6	160	159	160	160	160	159	159	159	159	160	160	160.2	160	160	160	160.4	186	150	149	119
7	45	44.4	44.2	44	44.4	44.2	44.1	44.1	44.2	44.2	44.2	44.2	44.1	44.1	44	44	77	40.6	41	27
8	104	103	102	101	101	100	100	99.7	99.7	99.7	99.6	99	99	99	98.6	98.4	127	91	89.8	57.5
9	77	75.9	77.5	80	78.1	76.4	76	76.6	77.5	78.2	78.8	79.8	78.5	77	75.7	75	102	69	70	48

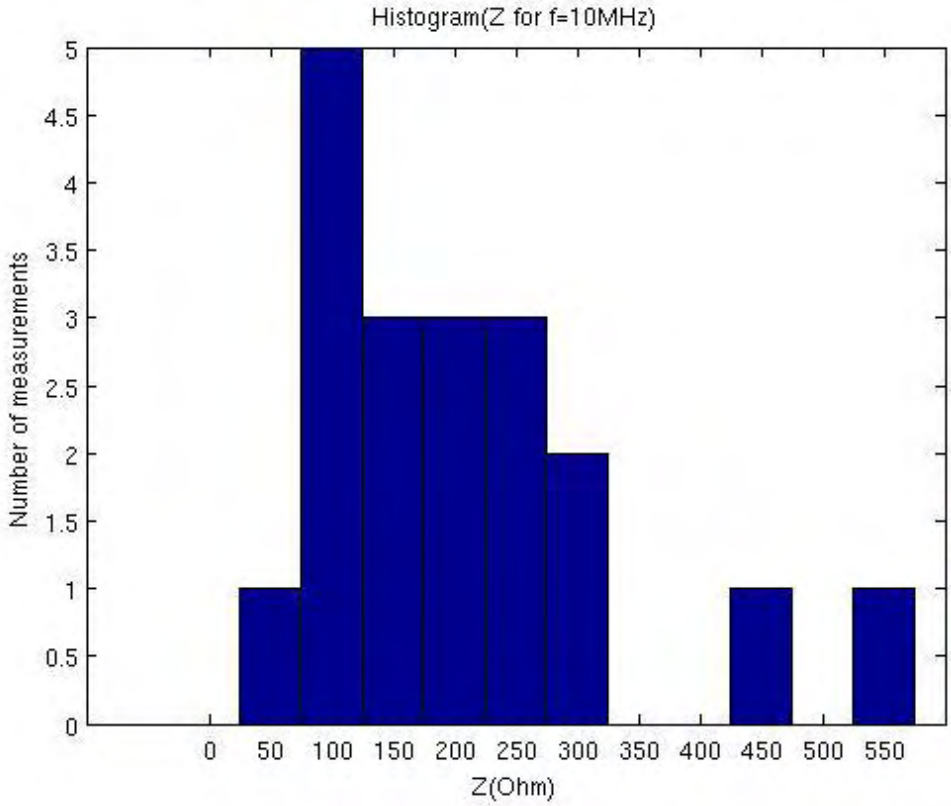
10	239	238	238	237	237	236	236	236	236	235	235	230	229	229	228	228	233	199	174	109
11	109	108	108	108	108	108	108	108	108	108	108	107.7	107	107.2	107	106	127	93	89	46
12	262	262	261	261	260	260	260	259	259	258	258	257	256	255	254	253	239	204	177	107
13	48	48	47	48	47.9	47	47.5	47.4	47	47	47	47	47	47	47	46.6	79	40	40.1	10
14	144	144	144	143	143	143	143	143	143	142.8	142	142	142	141	141	140	159	125	117	72
15	237	234	234	233	233	233	233	233	233	233	233	233	233	232	233	232	228	190	170	107
16	98	98.5	98.4	98.4	98	98	98	98	98	98	98	98	98	98	98	98	117	84	82	43
17	222	220	220	220	221	220	222	221	222	222	223	222	222	221	221	220	215	182	160	100
18	71	71	70	71	72	71	72	72	72	72	73	73	73	73	73	73	105	68	71	36
19	438	438	438	438	438	437	438	438	437	437	438	437	437	437	437	437	428	377	346	205

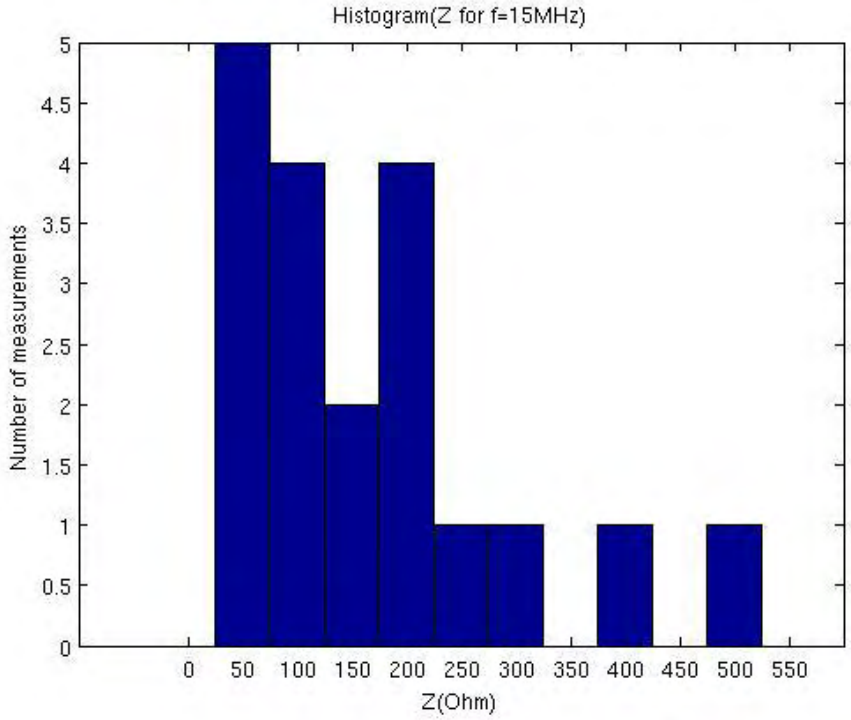



Histogram(Z for f=200KHz)
Number of measurements
Z(Ohm)
0
0.5
1
1.5
2
2.5
3
3.5
4
0
50
100
150
200
250
300
350
400
450
500
550


Histogram(Z for f=250,300,350,400,450,500,550,600,700,800,900kHz)
Number of measurements
Z(Ohm)
0
0.5
1
1.5
2
2.5
3
3.5
4
0
50
100
150
200
250
300
350
400
450
500
550

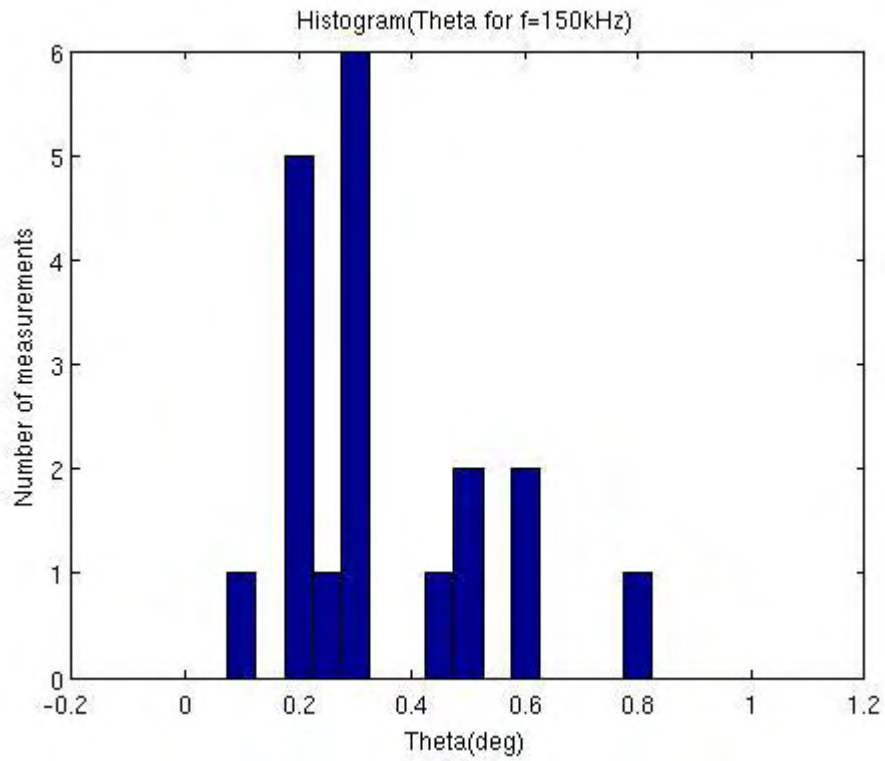

Histogram(Z for f=650kHz)
Number of measurements
Z(Ohm)
0
0.5
1
1.5
2
2.5
3
3.5
4
0
50
100
150
200
250
300
350
400
450
500
550

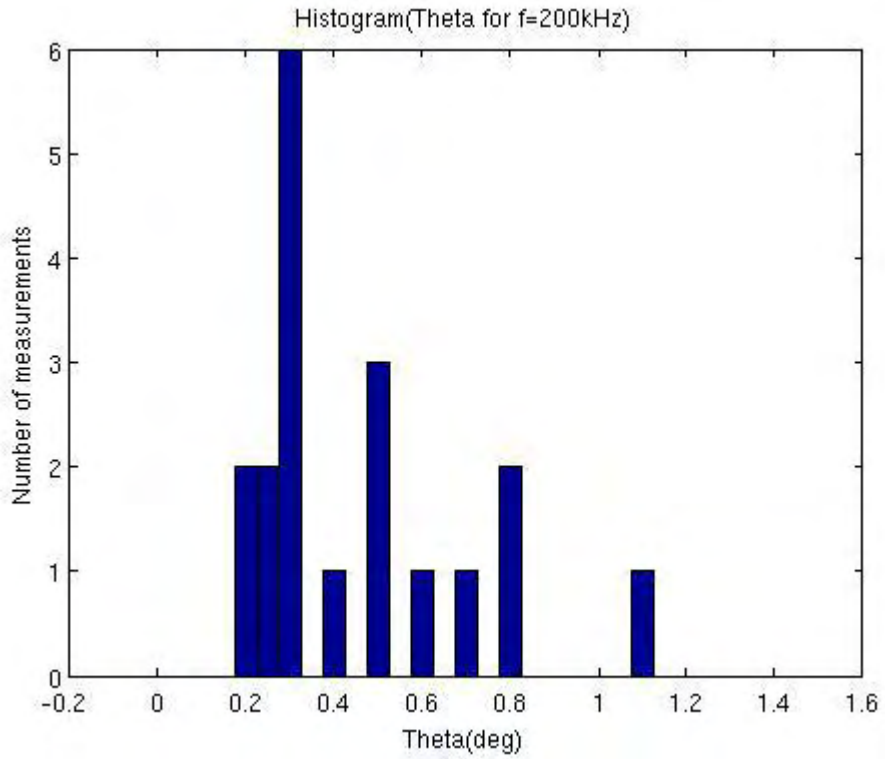

Histogram(Z for f=10MHz)
Number of measurements
Z(Ohm)
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
0
50
100
150
200
250
300
350
400
450
500
550

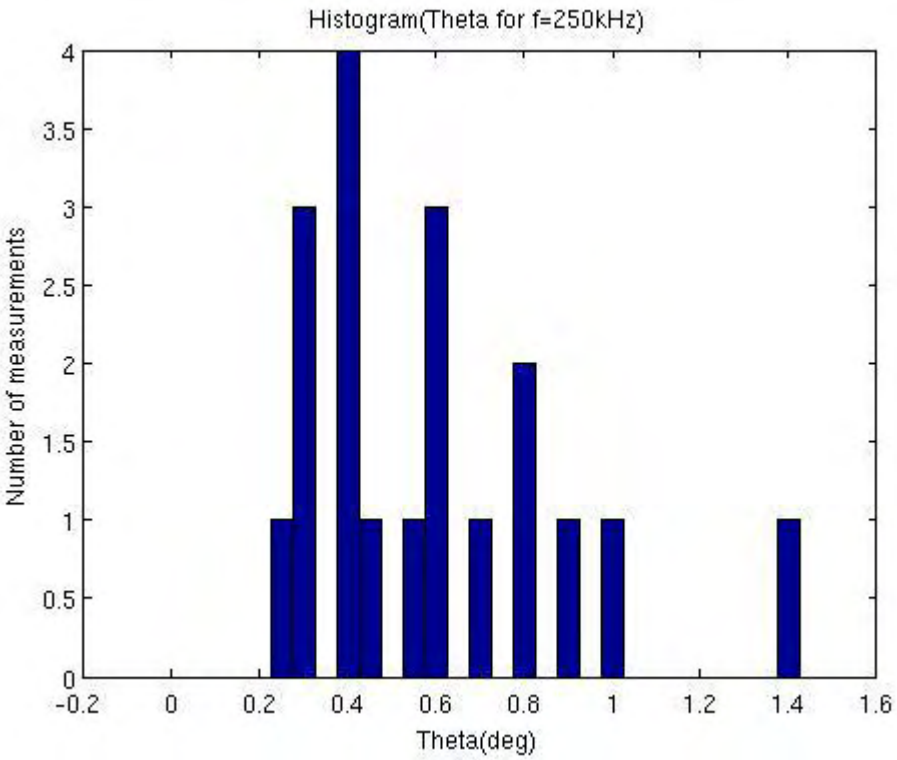

Histogram(Z for f=15MHz)
Number of measurements
Z(Ohm)
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
0
50
100
150
200
250
300
350
400
450
500
550

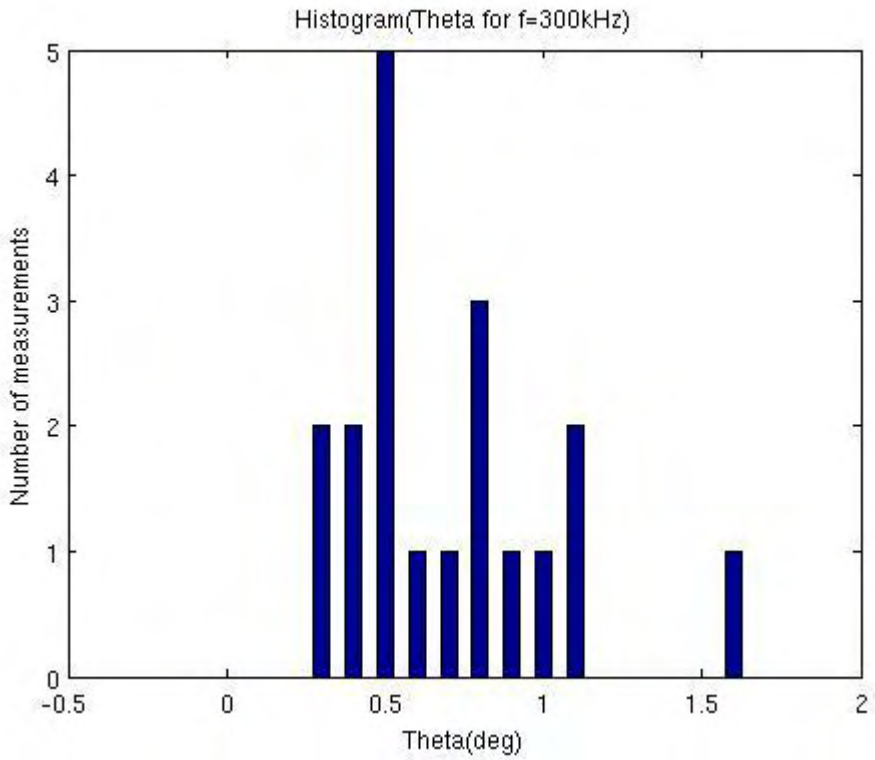
For Theta

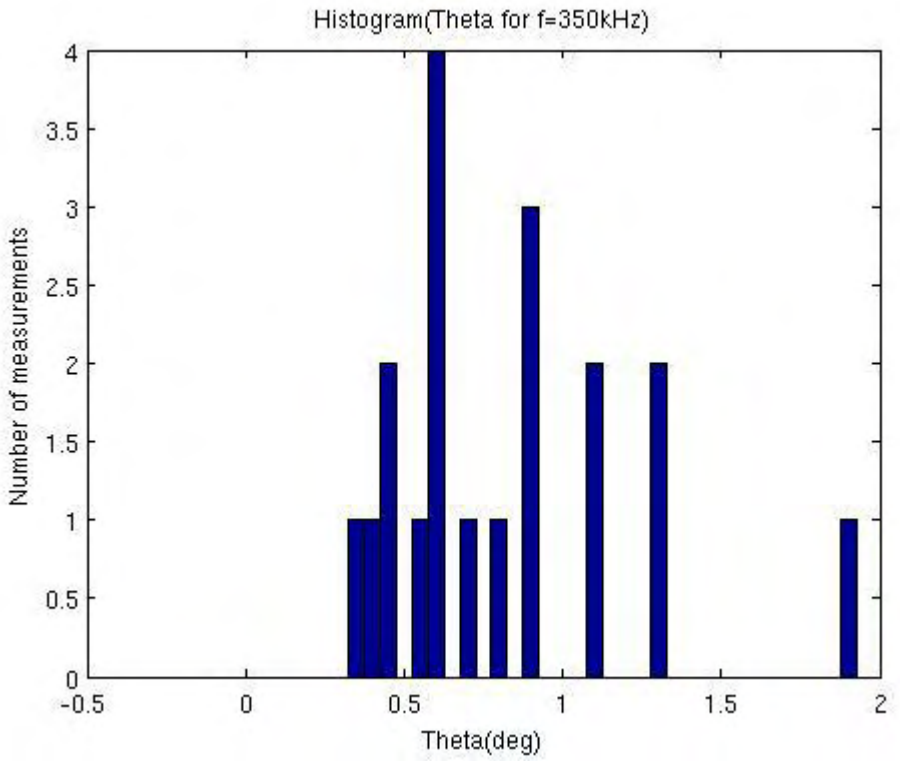
Fr /#	100 KHz	150 KHz	200 KHz	250 KHz	300 KHz	350 KHz	400 KHz	450 KHz	500 KHz	550 KHz	600 KHz	650 KHz	700 KHz	800 KHz	900 KHz	1 MHz	10 MHz	15 MHz	20 MHz	30 MHz
1	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1	1.1	1.2	1.3	1.5	1.7	1.6	9	16	13
2	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	0.9	1	1.15	1.2	1.4	1.4	1.7	0.5	8.2	15	13
3	0.13	0.2	0.26	0.3	0.3	0.45	0.51	0.57	0.6	0.7	0.7	0.8	0.8	0.9	1	1.1	1.5	5	12	11
4	0.2	0.3	0.3	0.55	0.6	0.7	0.8	0.9	1	1.1	1.2	1.2	1.3	1.5	1.6	1.8	24	5	14	23
5	0.1	0.3	0.3	0.4	0.48	0.53	0.59	0.62	0.68	0.74	0.8	0.87	0.9	1	1.1	1.23	4.5	9	14.7	21.9
6	0.12	0.2	0.25	0.3	0.4	0.45	0.5	0.57	0.6	0.7	0.7	0.8	0.9	1	1.14	1.3	4.8	8.5	12	20.1
7	0.08	0.1	0.2	0.26	0.3	0.37	0.4	0.5	0.57	0.62	1.01	1.1	1.18	1.3	1.5	1.67	19	12	19.5	30
8	0.08	0.1	0.2	0.26	0.3	0.37	0.4	0.5	0.57	0.62	0.7	0.7	0.8	0.9	1	1.16	9.5	8.4	15.3	25.4
9	0.19	0.3	0.3	0.44	0.5	0.6	0.8	0.8	0.9	1	1.1	1.16	1.3	1.56	1.8	2	9.5	16	24	37
10	0.3	0.45	0.5	0.7	0.8	0.9	1	1.2	1.3	1.4	1.5	1.6	1.7	1.9	2	2.2	1.7	10	21	7
11	0.4	0.6	0.8	1	1.1	1.3	1.5	1.6	1.8	1.9	2	2.2	2.3	2.5	2.7	2	5	14	26	35
12	0.5	0.8	1.1	1.4	1.6	1.9	2.1	2.3	2.5	2.7	2.9	3.1	3.3	3.6	3.9	4.2	7.8	20	31	23
13	0.3	0.5	0.7	0.8	1	1.1	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2	2.1	2.2	20	4.5	13.4	19
14	0.4	0.6	0.8	0.9	1.1	1.3	1.5	1.6	1.7	1.8	1.9	2	2.1	2.3	2.4	2.6	2.3	12.3	23	17
15	0.3	0.5	0.6	0.8	0.9	1.1	1.2	1.4	1.6	1.7	1.9	2	2.2	2.5	2.8	3	9	24	37	27
16	0.2	0.3	0.5	0.6	0.8	0.9	1	1.2	1.3	1.4	1.5	1.6	1.8	2	2.3	2.5	4.3	18	29	31
17	0.2	0.3	0.5	0.6	0.78	0.9	1	1.1	1.2	1.3	1.4	1.6	1.7	2	2.3	2.5	4.5	14	26	13
18	0.1	0.2	0.2	0.3	0.4	0.4	0.5	0.5	0.6	0.6	0.7	0.7	0.8	1	1.1	1.2	12	9.6	17	35
19	0.25	0.3	0.4	0.6	0.7	0.8	0.9	1.1	1.2	1.3	1.5	1.5	1.7	1.9	2.1	2.4	11	20	34	32

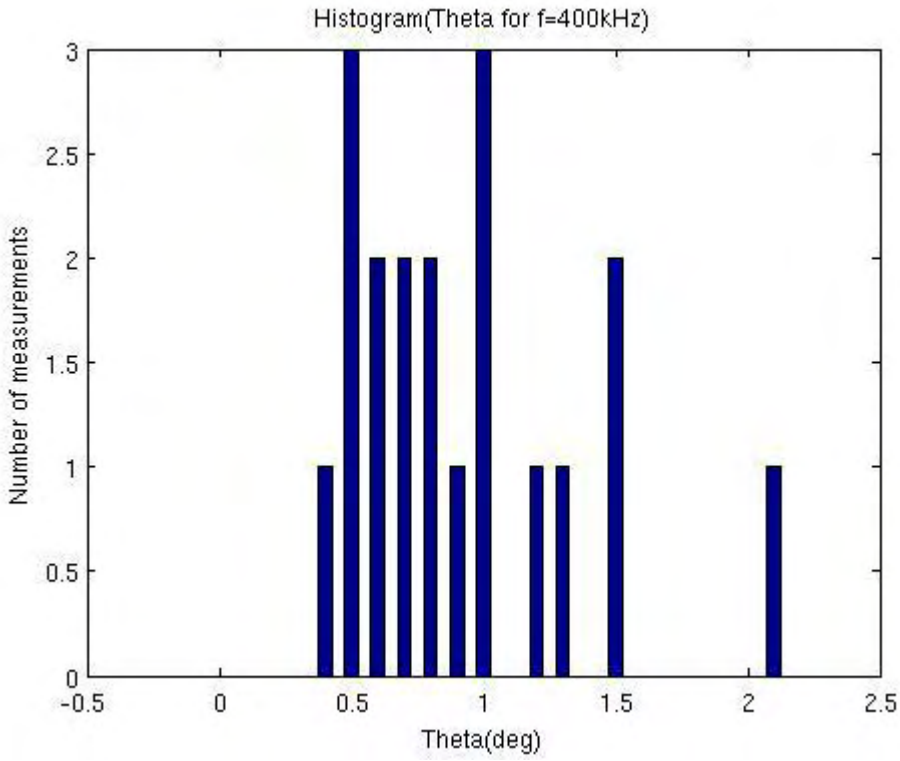

Histogram(Theta for f=150kHz)
Number of measurements
Theta(deg)
0
1
2
3
4
5
6
-0.2
0
0.2
0.4
0.6
0.8
1
1.2

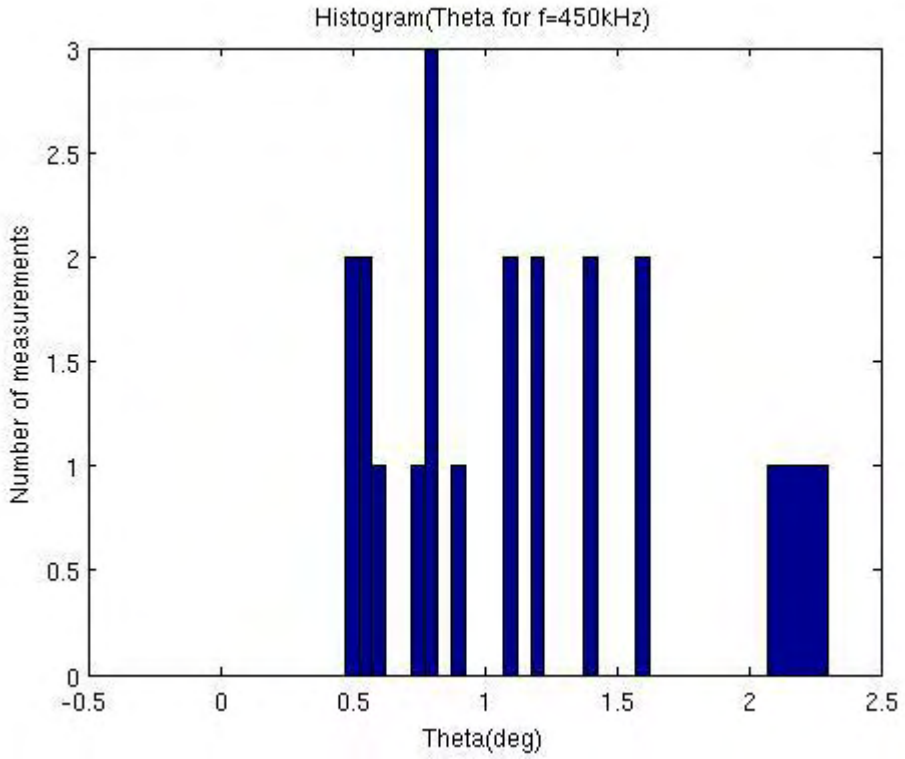

Histogram(Theta for f=200kHz)
Number of measurements
Theta(deg)
0
1
2
3
4
5
6
-0.2
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6

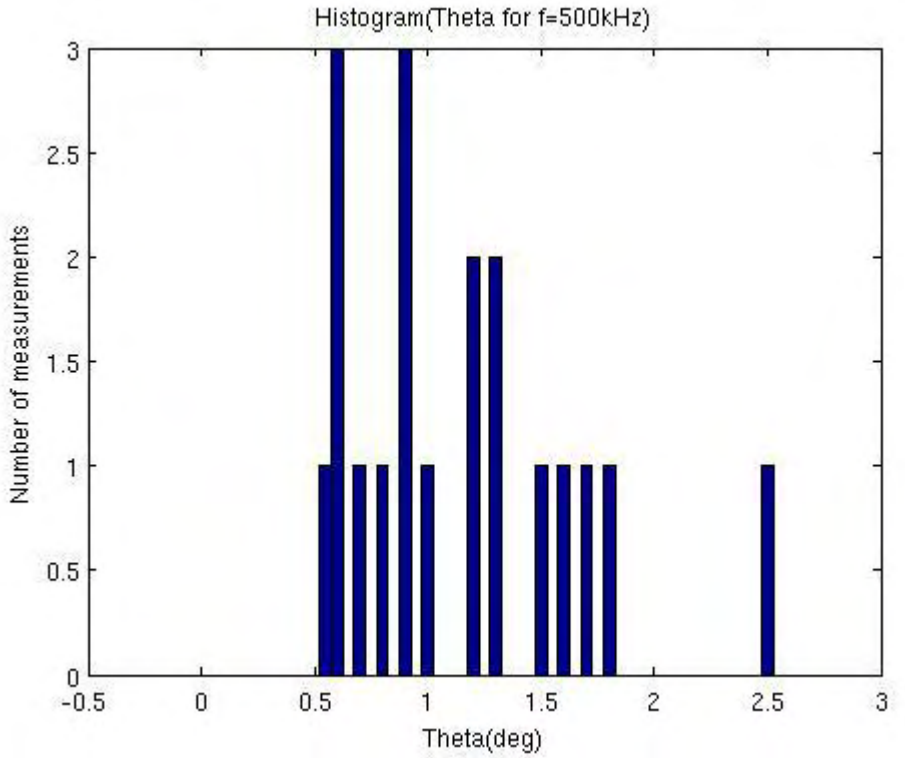

Histogram(Theta for f=250kHz)
Number of measurements
Theta(deg)
0
0.5
1
1.5
2
2.5
3
3.5
4
-0.2
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6

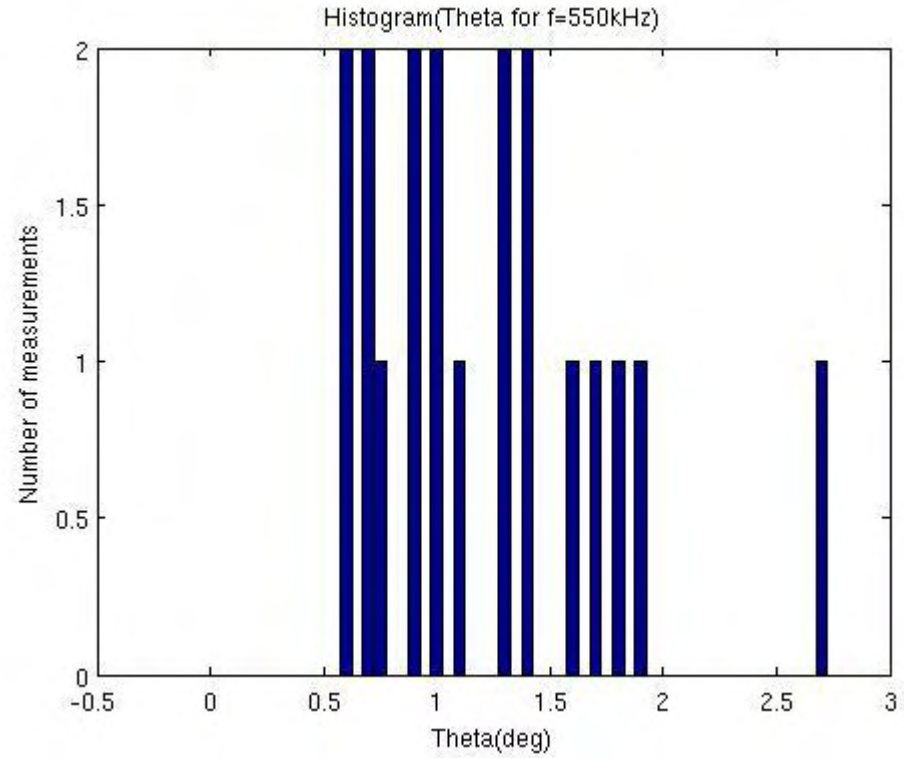

Histogram(Theta for f=300kHz)
Number of measurements
Theta(deg)
0
1
2
3
4
5
-0.5
0
0.5
1
1.5
2

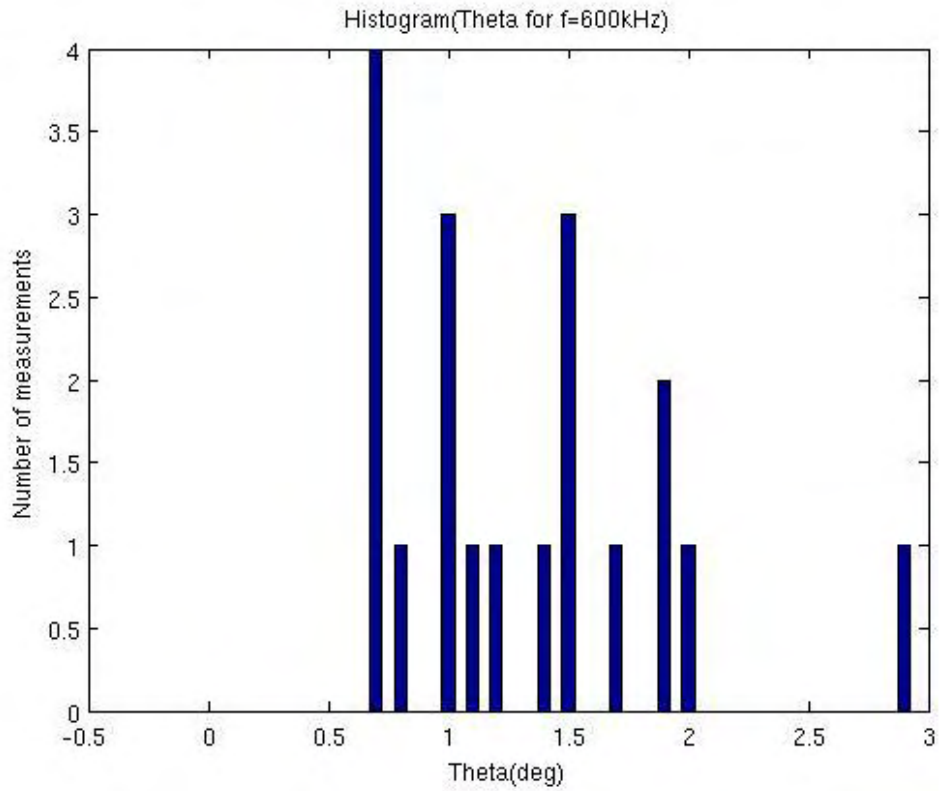

Histogram(Theta for f=350kHz)
Number of measurements
Theta(deg)
4
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2

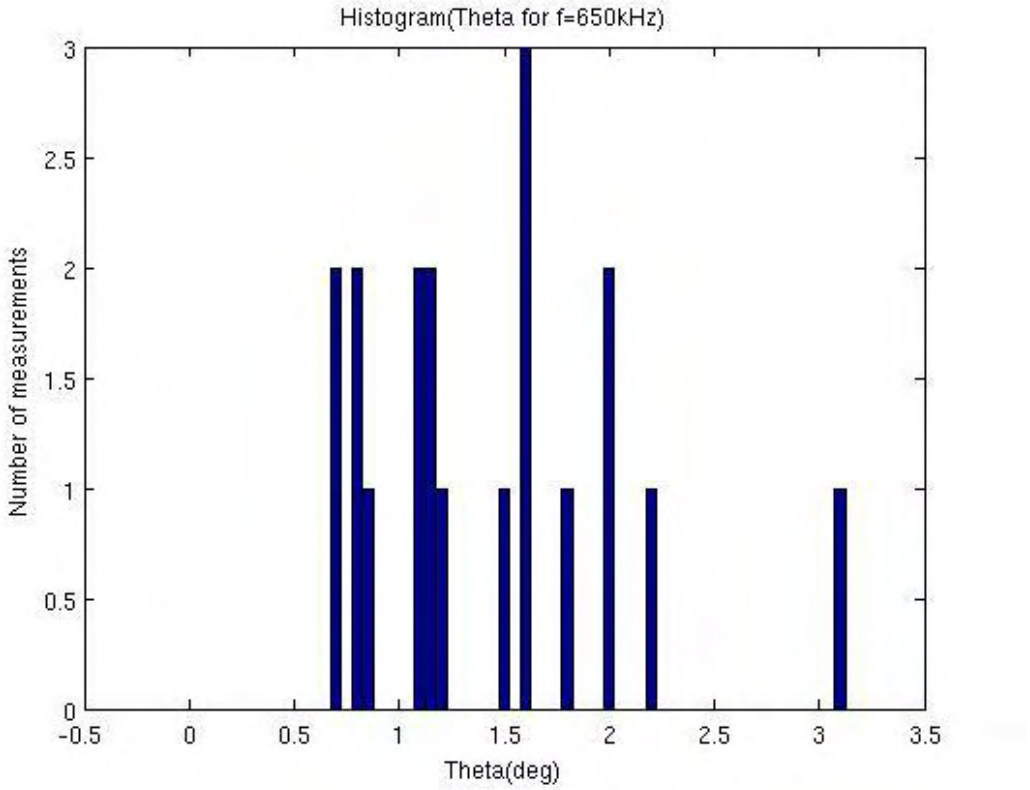

Histogram(Theta for f=400kHz)
Number of measurements
Theta(deg)
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5

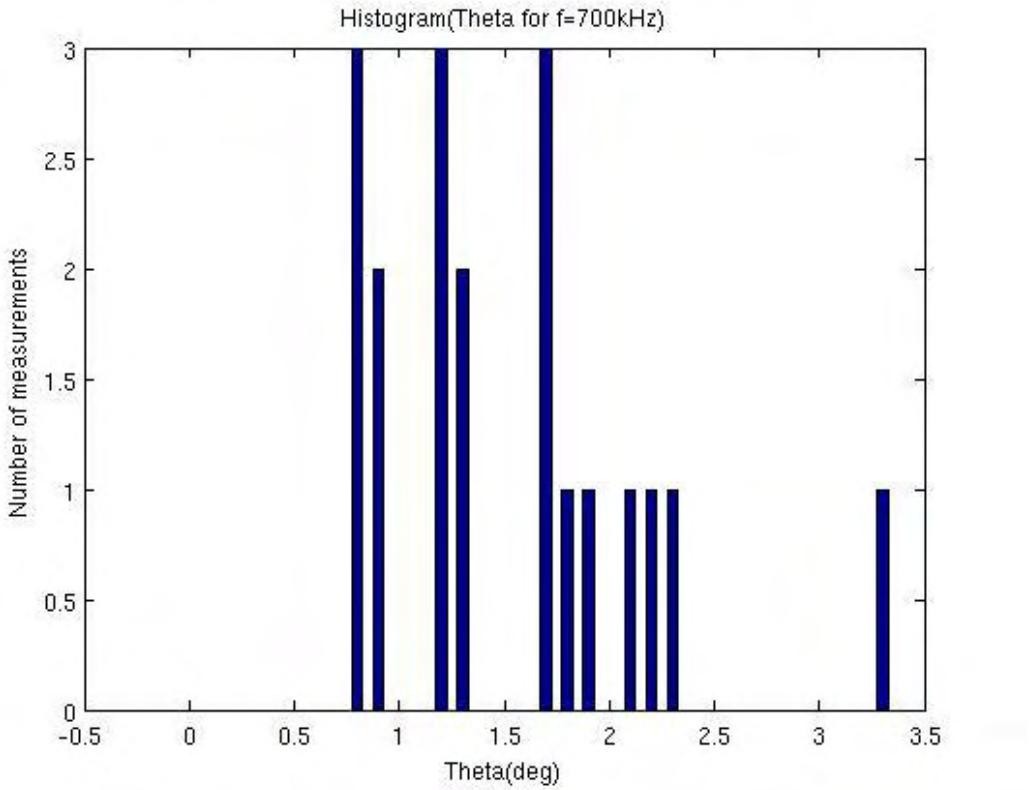

Histogram(Theta for f=450kHz)
Number of measurements
Theta(deg)
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5

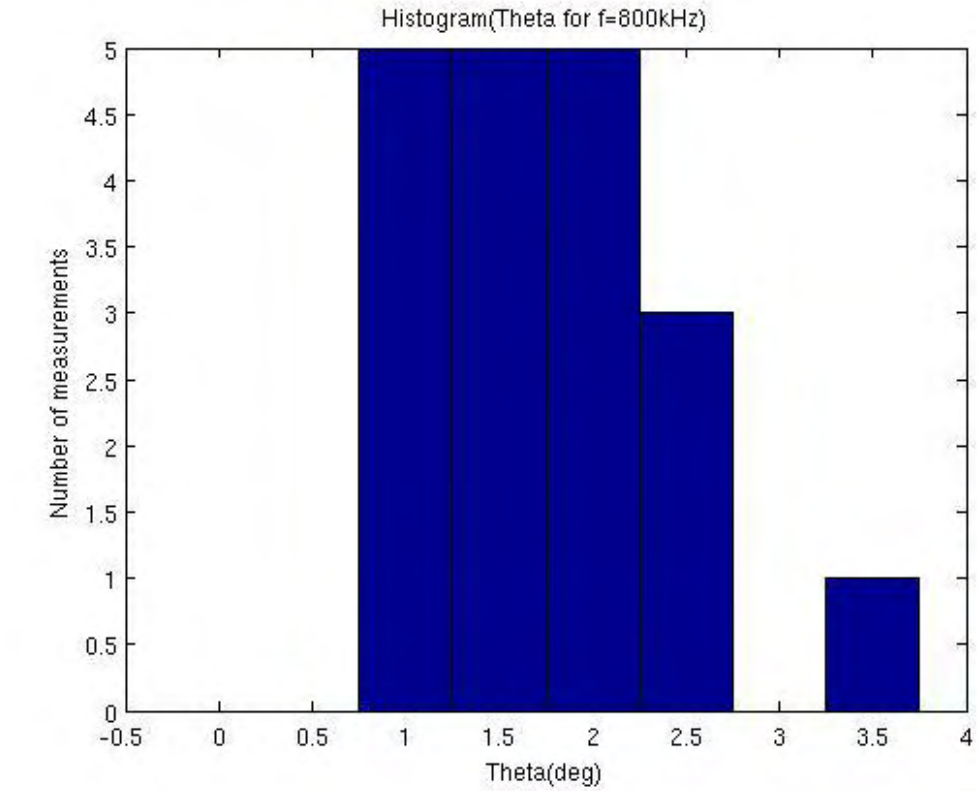

Histogram(Theta for f=500kHz)
Number of measurements
Theta(deg)
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5
3

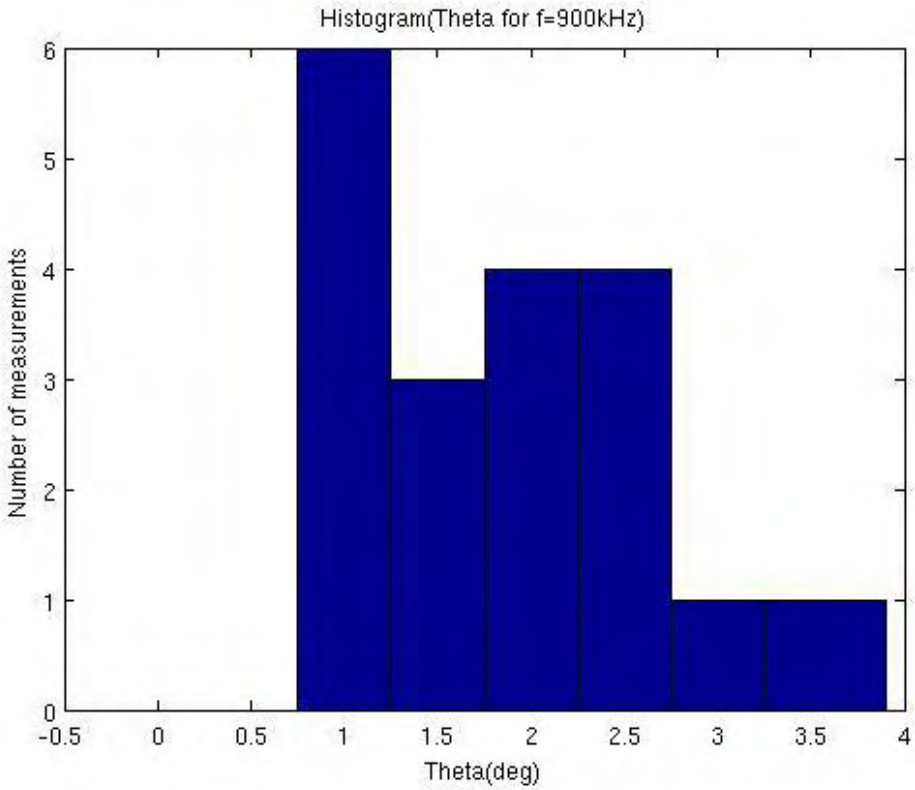

Histogram(Theta for f=550kHz)
Number of measurements
Theta(deg)
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5
3

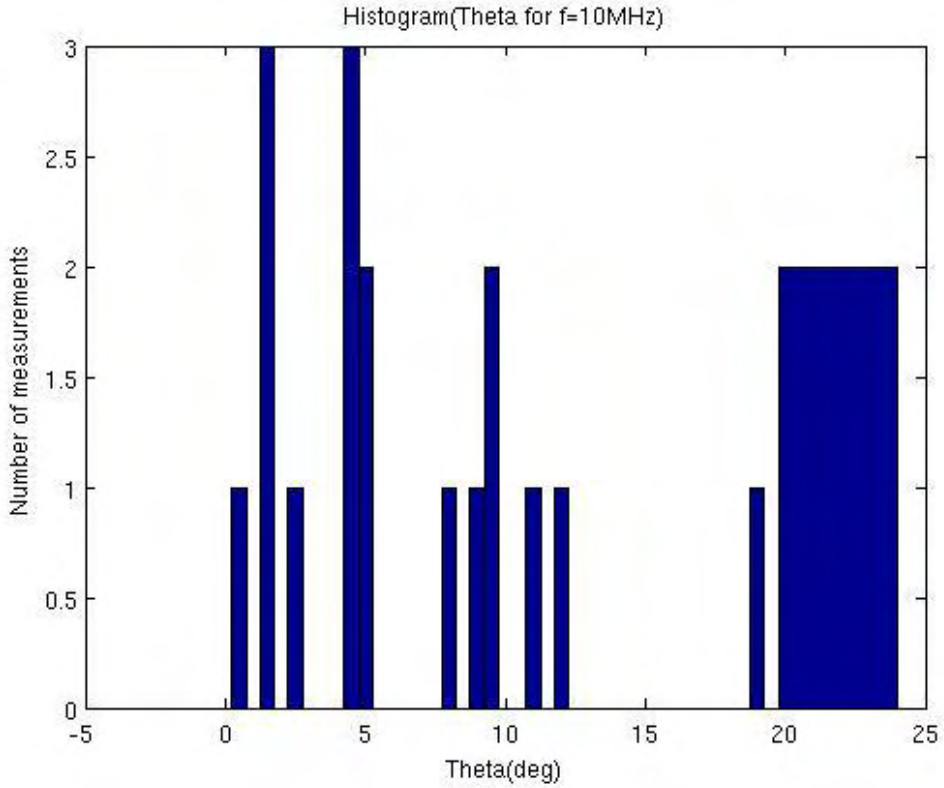

Histogram(Theta for f=600kHz)
Number of measurements
Theta(deg)
4
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5
3

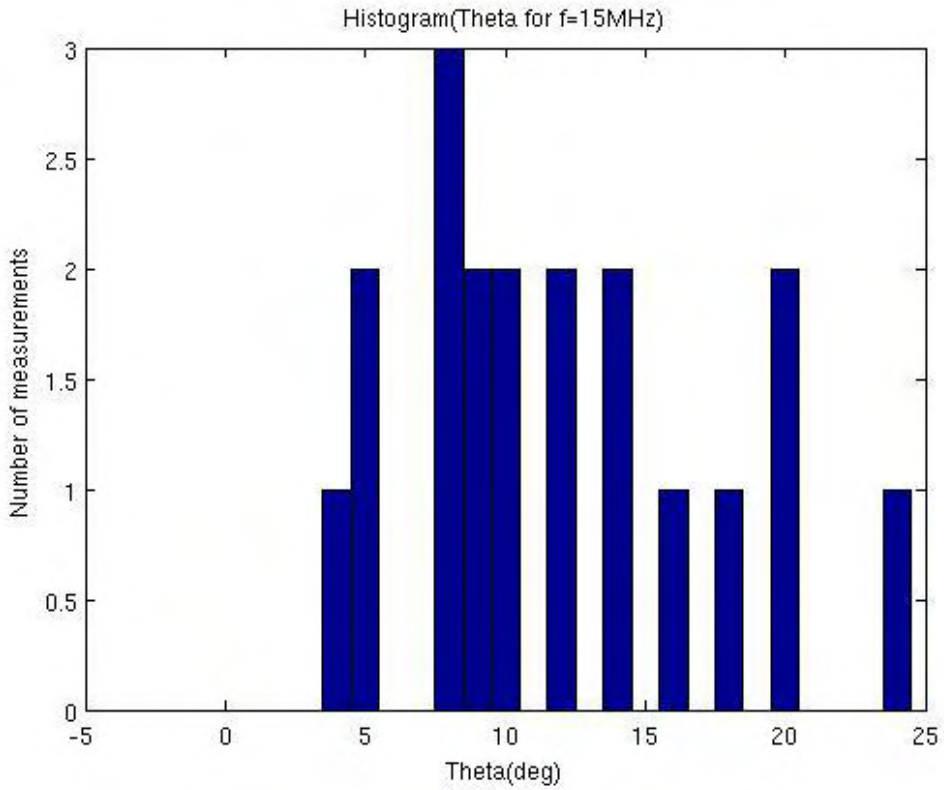

Histogram(Theta for f=650kHz)
Number of measurements
Theta(deg)
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5
3
3.5

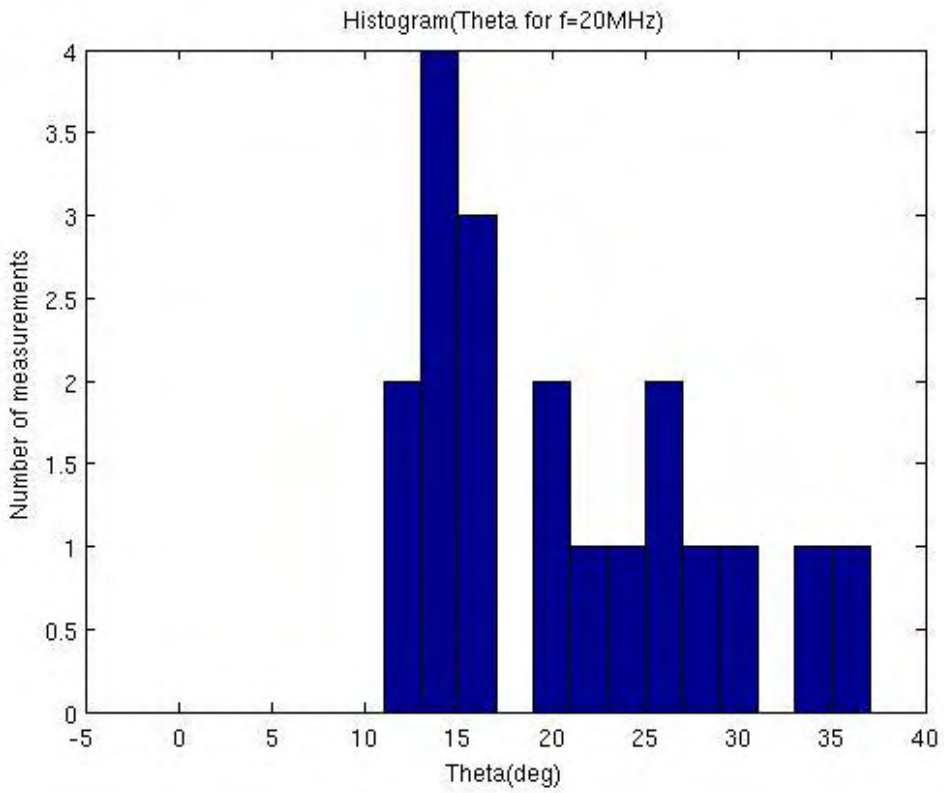

Histogram(Theta for f=700kHz)
Number of measurements
Theta(deg)
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5
3
3.5


Histogram(Theta for f=800kHz)
Number of measurements
Theta(deg)
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
1.5
2
2.5
3
3.5
4


Histogram(Theta for f=900kHz)
Number of measurements
Theta(deg)
6
5
4
3
2
1
0
-0.5
0
0.5
1
1.5
2
2.5
3
3.5
4


Histogram(Theta for f=10MHz)
Number of measurements
Theta(deg)
0
0.5
1
1.5
2
2.5
3
-5
0
5
10
15
20
25


Histogram(Theta for f=15MHz)
Number of measurements
Theta(deg)
0
0.5
1
1.5
2
2.5
3
-5
0
5
10
15
20
25


Histogram(Theta for f=20MHz)
Number of measurements
Theta(deg)
0
0.5
1
1.5
2
2.5
3
3.5
4
-5
0
5
10
15
20
25
30
35
40