UNIVERSITY OF THESSALY

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

DUAL MODE CHARGE PUMP BASED DC-DC CONVERTER

Diploma Thesis

Moustakas Vasileios

Supervisor: Plessas Fotios

September 2023

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ΠΑΝΕΠΙΣΤΗΜΙΟ ΘΕΣΣΑΛΙΑΣ

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Διπλωματική Εργασία

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Moustakas Vasileios

Diploma Thesis

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Moustakas Vasileios

Abstract

This Thesis introduces the design of a dual-mode inductorless charge pump (CP) employing a fractional architecture with buck-boost capabilities. The proposed design uses various capacitor arrangements within a cross-coupled model to generate fractional voltage ratios including ($\frac{1}{3}$,$\frac{1}{2}$,$\frac{2}{3}$,$\frac{3}{2}$,$\frac{2}{1}$) in order to allow for a wide selection of voltage options. This configuration aims to minimize the area on the die while preserving high efficiency and low ripple. The proposed charge pump has been designed using IHP 130nm metal-oxide-semiconductor (CMOS) technology and has been simulated in Cadence Virtuoso.

Keywords:

charge pumps, buck-boost, cross-coupled, CMOS,

Διπλωματική Εργασία

ΜΕΤΑΤΡΟΠΕΑΣ DC-DC ΔΙΠΛΗΣ ΛΕΙΤΟΥΡΓΙΑΣ ΒΑΣΙΣΜΕΝΟΣ ΣΕ ΑΝΤΛΙΑ ΦΟΡΤΙΟΥ

Μουστάκας Βασίλειος

Περίληψη

Αυτή η Διατριβή παρουσιάζει τον σχεδιασμό μιας διπλής λειτουργίας αντλίας φόρτισης (CP) που χρησιμοποιεί έναν κλασματικό σχεδιασμό με δυνατότητες buck-boost. Ο προτεινόμενος σχεδιασμός χρησιμοποιεί διάφορες διατάξεις πυκνωτών μέσα σε ένα cross-coupled μοντέλο για τη δημιουργία κλασματικών αναλογιών τάσης, συμπεριλαμβανομένων ($\frac{1}{3}$,$\frac{1}{2}$,$\frac{2}{3}$,$\frac{3}{2}$,$\frac{2}{1}$) προσφέροντας ένα ευρύ φάσμα επιλογών τάσης. Αυτή η διαμόρφωση στοχεύει στο να ελαχιστοποιήσει το εμβαδόν στο ενσωματωμένο κύκλωμα διατηρώντας ταυτόχρονα υψηλή αποδοτικότητα και χαμηλή διακυμανση στην ταση εξοδου. Η αντλία φόρτισης έχει σχεδιαστεί χρησιμοποιώντας την τεχνολογία μεταλλικού-οξειδίου-ημιαγωγών (CMOS) 130nm της IHP και έχει υποστεί προσομοίωση στο Cadence Virtuoso.

Λέξεις-κλειδιά:

Αντλία φόρτισης, buck-boost, cross-coupled, CMOS

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Abbreviations

CP	Charge Pump
CMOS	complementary metal-oxide semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor

Chapter 1

Introduction

Over the last decades, the field of electronics has witnessed an immense evolution, and with the world struggling to keep up with the power consumption demands, energy efficiency has become one of the main challenges of the field. As of September of 2023, [4] there are over 11.856 Billion mobile connections worldwide. In these highly energy-demanding conditions power management devices such as Charge pump DC-DC converters are emerging as one of the most important circuits of our electronic age.

Charge pumps rely on clever manipulation of capacitors and transistor switches in order to increase or decrease the voltage, replacing transformers and inductors reducing the cost and the area on the die. As a result, these circuits aim to provide longer-lasting batteries and slimmer devices.

But the importance of Charge Pumps doesn't end there. The world has entered the IoT era, where Billions of devices continuously exchange data, and energy efficiency has become an imperative need. IoT sensors are found everywhere in our day-to-day life from smart homes and wearable devices to environmental monitors. In order for these sensors to function for years on a single charge they rely on energy harvesting from solar energy, radio waves, or even vibrations. Charge pumps play a crucial role in managing, and converting the energy needed for the sensors to work as intended.

1.1 Thesis Scope

Nowadays in the chase of energy efficiency power management circuits have evolved in order to provide a wide range of solutions such as voltage regulation, voltage conversion

(charge pumps), battery management, and energy harvesting. These devices aim to prolong battery life and ensure stable reliable operation. In this thesis, we will focus on voltage conversion circuits, specifically charge pumps. Various topologies of DC-DC charge pump converters have been proposed in order to responsibly deliver a stable and efficient power supply to different parts of an electronic system. However, with the ever-rising complexity of electronic systems precise voltage regulation is needed in order to maximize energy efficiency.

The objective of this Thesis is to demonstrate a state-of-the-art buck-boost fractional cross-coupled charge pump in order to provide high adaptability in circuits with non-standard voltage levels such as battery-powered devices, reduce the die area when used in Integrated circuits to provide internal voltage levels required by different parts of the chip and the ability to optimize for specific loads conditions. Cadence's Virtuoso was utilized to create and simulate a charge pump that uses flying capacitors in a cross-coupled configuration with a selection circuit in order to provide five different voltage fractions.

1.1.1 Contribution

The contribution of this thesis is summarized as follows:

1. A review was conducted on charge pump topologies
2. An analysis was operated on power loss in switched capacitor power converters
3. A state-of-the-art charge pump was implemented and simulated in Cadence's Virtuoso

1.2 Volume Structure

This thesis is structured into five chapters, each chapter provides the reader with the necessary knowledge to progress into the next chapter. Chapter 2 analyzes the basic working principle of current charge pump topologies. Chapter 3 focuses on the efficiency and the Power Loss in Switched-Capacitor topologies providing a mathematical analysis. Chapter 4 presents a detailed analysis of the case study, addressing the central problem of the thesis and providing a state-of-the-art topology to solve it. Chapter 5 explores the results of the proposed charge pump. Finally, Chapter 6 summarizes the findings and discusses potential future improvements.

Chapter 2

Switched Capacitance Converter Topologies and Fundamentals

2.1 Introduction

This chapter dives into the basic principles of charge pumps. Starting with the charge transfer between capacitors and analyzing the basic charge pump topologies and their evolution from the diode Dickson to the cross-coupled charge pump.

2.2 Principle of Charge Transfer

The working principle of charge pumps is the periodic charge transfer between capacitors, so in order to understand it it's necessary to first understand the concept of charge distribution between two capacitors. Let's contemplate two capacitors C1 and C2, charged to V1 and V2, respectively as shown in Fig 2.1. This voltage difference results in the creation of an electric field E_i between the plates of these capacitors as shown in equation 2.1.

$$\vec{E_i} * d_i = V_i (i = 1, 2) \tag{2.1}$$

In equation 2.1 d_i is the distance between the plates of the capacitor C_i. When the switch closes a potential difference between the capacitors results in the redistribution of charges. This phenomenon is accomplished by an electrostatic force F as shown in equation 2.2

$$W = -\int \frac{\vec{E}}{q} * \vec{d_s} \; = -\int \vec{F} * \vec{d_s} \tag{2.2}$$

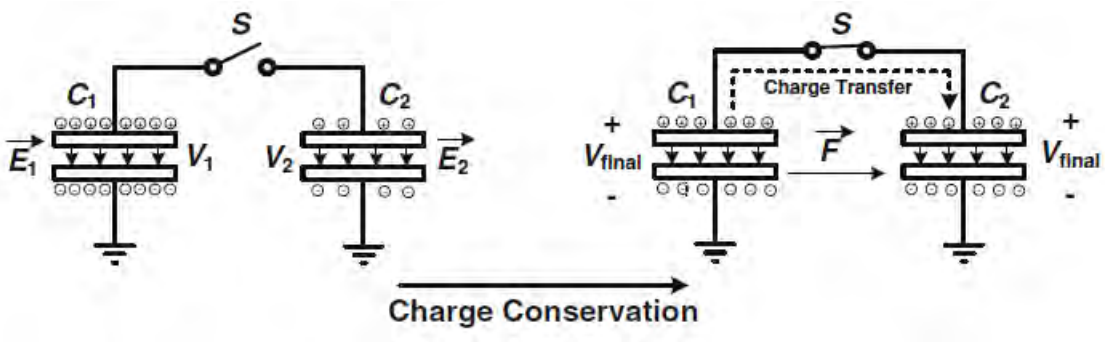

Figure 2.1: Charge transfer between capacitors [1]

Where W represents the work on the stored charges due to the voltage difference as shown in equation 2.3, q is the charge, and F is the electrostatic force on the charge along d_s. Let us consider $V_1 > V_2$ in the equations 2.2 and 2.3. We get 2.4

$$\vec{E_i} * d_i = V_i (i = 1, 2) \tag{2.3}$$

$$V_1 - V_2 = \frac{W}{q} = -\int \vec{F} * \vec{d_s} \tag{2.4}$$

Equation 2.4 shows that as a voltage difference exists among the capacitors, an electrostatic force redistributes the stored charges until the voltage of both capacitors is equal. The final voltage value of its capacitor is based on the application of the conservation of charge principle, which states that when two capacitors are connected in parallel the total charge is equal to the sum of the original charges of the capacitors as shown in 2.5.

$$Q_{total} = C_1 V_1 + C_2 V_2 \tag{2.5}$$

When the two capacitors reach the same voltage, by solving Equation 2.5 we get 2.6.

$$V_{final} = (\frac{C_1}{C_1 + C_2}) V_1 + (\frac{C_2}{C_1 + C_2}) V_2 \tag{2.6}$$

Let's consider a basic voltage replicator charge pump depicted in figure 2.2. Capacitor C1 is the pumping capacitor while C2 is the output capacitor both initially charged to zero volts. Firstly, during the charge cycle switch S1 closes charging C1 to VDD, then during the discharge cycle C2 closes resulting in the parallel connection between the capacitors. Ideally after the first cycle, the output capacitor is charged to V_{out1} as shown in the equation 2.7.

$$V_{out1} = (\frac{C_1}{C_1 + C_2}) V_{DD} \tag{2.7}$$

During the second cycle, the pumping capacitor is charged to VDD once more during the charge phase and redistributes the charge to the output capacitor in the discharge phase. The output voltage after two cycles can be seen in 2.8.

$$V_{out2} = (\frac{C_1}{C_1 + C_2})V_{DD} + (\frac{C_2}{C_1 + C_2})V_{out1} \tag{2.8}$$

While the voltage replicator can only charge the output capacitor to the input voltage, other charge pump topologies using the same concept can produce a wide range of higher and lower output voltages.

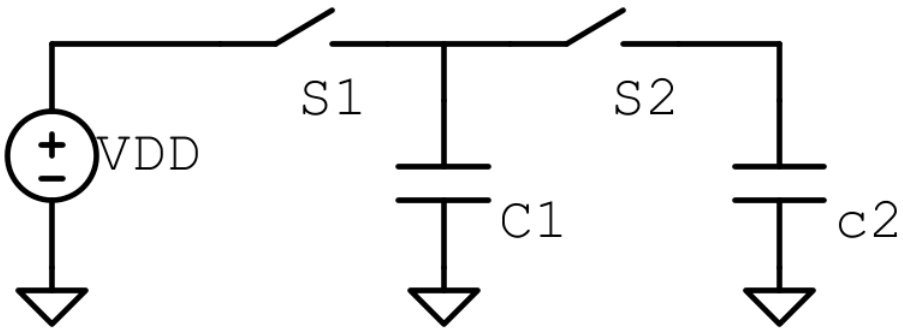

Figure 2.2: Basic Voltage Replicator Charge Pump

2.3 Fundamental Charge pump topologies

2.3.1 Diode Dickson charge pump

One of the most famous charge pump topologies was first demonstrated by Dickson in 1976 and is named after him [5]. As shown in figure 2.3 this topology employs diodes as self-timed switches with a forward bias voltage and a stray capacitance $V_D * C_S$ respectively. The circuit utilizes two anti-phase clocks CLK1 and Clk2 with a voltage amplitude of V_{DD}. During each clock cycle the the capacitors along the diode chain are charged and discharged. Let us consider the clock CLK1 to be high then the voltage at node 1 becomes $V_{DD} + V_{CLK1} - V_D$ this causes the diode D2 to conduct unlit the voltage at node 2 becomes $V_{DD} + V_{CLK1} - 2V_D$) then CLK1 drops to low and CLK2 switches to VDD resulting in the increase of node 2 to

$V_{DD} + 2 * (V_{CLK1} - V_D)$ [6]. This sequence occurs in the entirety of the chain and after N stage the output voltage has a value of equation 2.9.

$$V_{OUT} = V_{DD} + N * (V_{CLK1} - V_D) - V_D \tag{2.9}$$

While equation 2.9 provides a good understanding of the final output voltage it doesn't take into account the stray capacitance of the chain which reduces the output voltage by a factor of $\frac{C}{C + C_S}$. As a result, the output voltage after taking into account the stray capacitance is shown in equation 2.10.

$$V_{OUT} = V_{DD} + N * ((\frac{C}{C + C_S})V_{CLK1} - V_D) - V_D \tag{2.10}$$

Until now it has assumed that no load is present on the output of the charge pump. When the charge pump has to deliver a load I_{OUT} the output is reduced by $\frac{N * I_{OUT}}{(C + C_S) * f_s}$ which indicates that the output voltage is directly proportional to the operating frequency of the clock f_s. The output voltage after taking into consideration the load on the circuit becomes

$$V_{OUT} = V_{DD} + N * ((\frac{C}{C + C_S})V_{CLK1} - V_D - \frac{I_{OUT}}{(C + C_S) * f_s}) - V_D \tag{2.11}$$

Finally, charge pumps operate in two phases the charge and the discharge phase. When Clk1 is high charge is delivered to the output capacitor, while Clk2 is high the output capacitor delivers charge to the load. This leads to a phenomenon called ripple at the output. By considering an output resistance R_{OUT} the ripple voltage is given by 2.12.

$$\Delta V_{OUT} = \frac{V_{OUT}}{R_{OUT} * C_{OUT} * f_s} \tag{2.12}$$

It is observed that the ripple effect can be mitigated by increasing the frequency of the clocks or by using a larger output capacitor. But in the case of the larger capacitor, the circuit would take longer to reach its steady state.

2.3.2 CMOS Switch Dickson charge pump

The main advantage of the diode Dickson charge pump is the absence of control signals for the switches. However the unavailability of isolated diodes in semiconductor processes

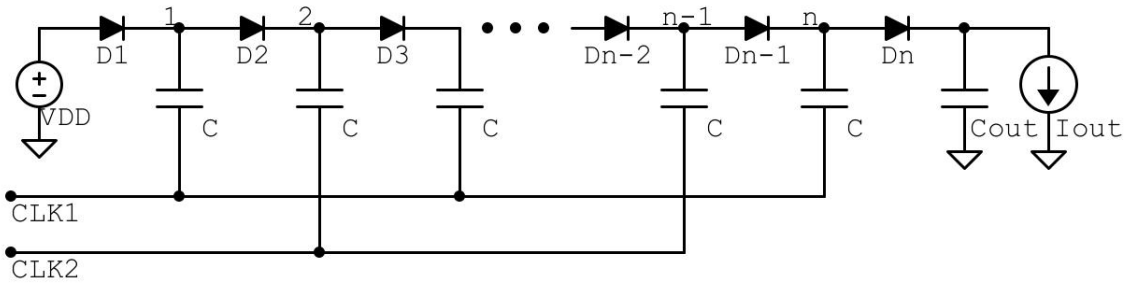

Figure 2.3: Diode-based Dickson Charge Pump

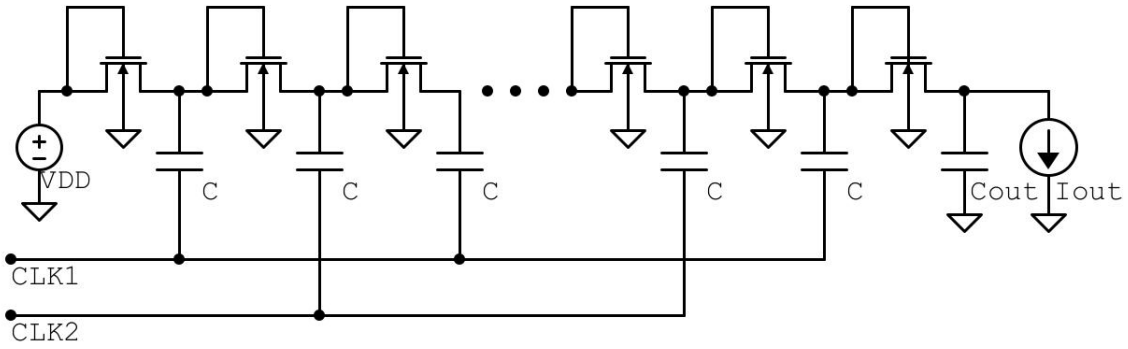

Figure 2.4: CMOS-based Dickson Charge Pump

and the reduction in the output voltage V_{OUT} due to the voltage drop from the diode's threshold V_D are major disadvantages. In order to address those challenges a CMOS-based implementation is demonstrated in Figure 2.4 with diode-connected NMOS transistors. Although replacing the diodes solved the unavailability of isolated diodes the voltage drop V_D is now replaced with the threshold voltage of the NMOS transistors as shown in equation 2.13. As the voltage of the power supply decreases so does the voltage of the clocks, consequently the pumping gain 2.14 reduces as well. It is clear from equations 2.13 2.14 that this topology is not suited for low-voltage design. Furthermore, the Bulk terminals of the Nmos transistor are connected to ground, while the source voltage of its transistor varies. Thus due to the body effect the threshold of its transistor is not the same and the threshold voltage increases with every passing stage of the chain making the topology even less efficient.

$$V_{OUT} = V_{DD} + N * ((\frac{C}{C + C_S})V_{CLK1} - V_{tn} - \frac{I_{OUT}}{(C + C_S) * f_s}) - V_{tn} \tag{2.13}$$

$$G_V = (\frac{C}{C + C_S})V_{CLK1} - V_{tn} - \frac{I_{OUT}}{(C + C_S) * f_s} \tag{2.14}$$

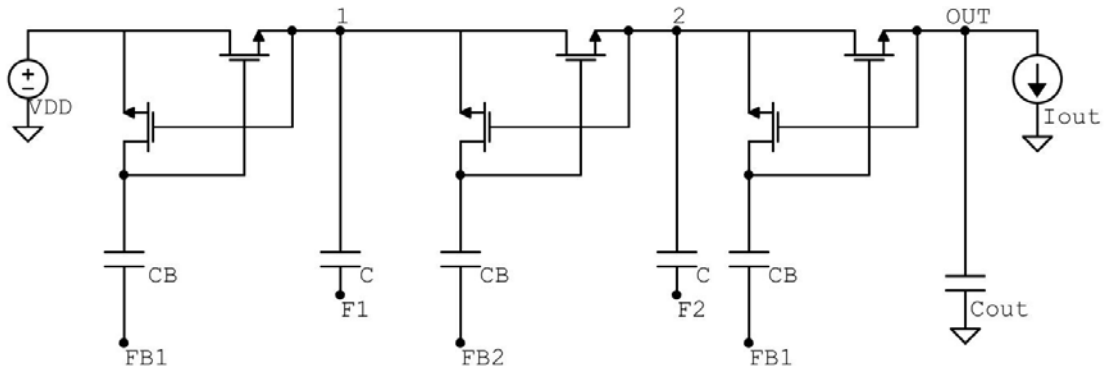

Figure 2.5: Bootstrap Dickson Charge Pump

2.3.3 Bootstrap Dickson charge pump

The main challenge of the Dickson charge pumps is the design of an efficient CMOS switch for the chain. Although creating a CMOS switch is a straightforward concept in this scenario the difficulty lies in the fact that the voltage of the drain and source terminals of the diode-connected transistors are higher than the voltage of the power supply. Especially in scenarios where the voltage generated in the next stage is used to control the previous stage, this creates problems in the start-up procedure when the voltages in the next stage are lower than those in the previous stage. One well-known solution to these challenges is called the Bootstrap switch Dickson charge pump 2.5. The Bootstrap circuit employs an extra supporting capacitor C_B and a CMOS transistor M_B at each stage in order to obtain the required high gate voltages.

Let's consider a single-stage bootstrap in order to understand its working principle 2.6. During the charge stage, Fb1 is low causing the transistor Mpass to be deactivated. However, the clock F1 is high causing the transistor MB to be active since its V_{GS} is 2VDD. Hence the capacitor CB is charged to 2.15 where ΔV represents the voltage transmission from one stage to the next when Mpass is active. During the pump stage, F2's voltage is at VDD while F1's is at zero resulting in the voltage of M_{pass} being increased significantly causing it to activate enabling the transfer of charge from j-1 to j. Although Bootstrap is an efficient topology that solves many of the previously mentioned challenges it has its own drawbacks. First of all, the voltage requirement of $2V_{DD}$ for the clocks has to be produced from a second charge pump or the input voltage must be reduced to $V_{DD}/2$ essentially making the $2V_{DD}$ that the clocks need the starting V_{DD}. Furthermore, this solution is only viable on multi-stage Bootstrap charge pumps because by cutting down the input voltage in half the output voltage will be V_{DD} so

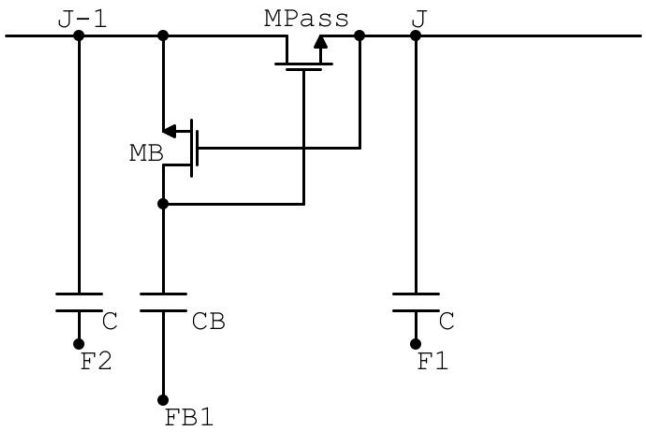

Figure 2.6: Single stage Bootstrap Dickson Charge Pump

more stages are needed to reach the needed result.

$$V_{i-1} = (i-1)VDD - (i-2)\Delta V \tag{2.15}$$

2.3.4 Cross coupled charge pump

The main disadvantage of Dickson charge pumps is the drop in the output voltage due to the threshold of the MOSFET switches which causes a significant efficiency drop. Hence in order to increase the efficiency and reduce the switching and conduction loss 3 is proposed by [7] that offers a small number of transistors and high efficiency levels called the cross-coupled charge pump 2.7. Let's consider a steady state in order to understand the working principle of the cross-coupled charge pump. In the first half period $CLK1 = V_{DD}$ and $CLK2 = 0$ thus V1 and V2 voltages are equal to $2V_{DD}$ and $Vout - V_{DD}$ respectively. Hence the transistors N2 and P1 controlled by V1 and V2 respectively are turned on resulting in the charging of pumping capacitor C2 by the input source and in the charge transfer between the capacitor C1 and C_{out}. After the first half period ends the voltage on C2 will reach V_{DD} and the voltage on C1 will have a value of $Vout - V_{DD}$. Similarly, the transistors P2 and N1 will be turned on in the second half period. Let's consider that both pumping capacitors are equal then the output voltage of the cross-coupled charge pump will be 2.16. Where C_p is the value of the pumping capacitors R_{out} the output resistance and T_s the switching period of the charge pump. It is clear that with a large switching frequency, low load, and large pumping capacitors the voltage at the output gets really close to $2V_{DD}$. It is important to mention that this topology can be used as a buck converter as well 4 by swapping the input and output terminals.

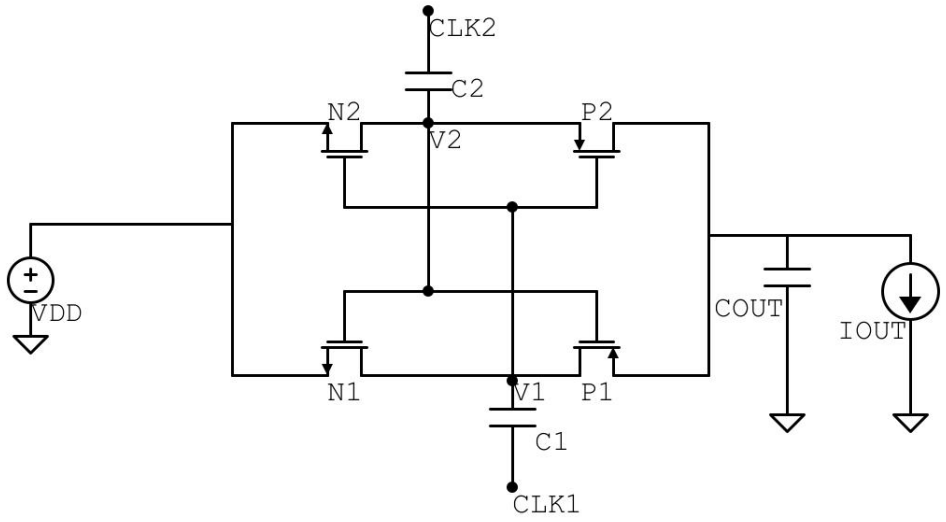

Figure 2.7: Cross-Coupled Charge Pump

$$V_{out} = \frac{2V_{DD}}{1 + \frac{T_s}{2RoutCp}} \tag{2.16}$$

Chapter 3

Analysis of Power Loses in Switched-Capacitor topologies

When designing power management circuits the main challenge is energy efficiency. In general, the energy efficiency of a power management DC-DC converter namely charge pumps is characterized as

$$\eta = \frac{P_{out}}{P_{out} + Ploss} * 100\% \tag{3.1}$$

Where P_{out} is the output power and P_{loss} is the power lost in the charge pump. It's clear that when losses are minimized the efficiency will be maximum. The four main loss factors when designing a charge pump are redistribution, conduction, reversion, and Switching Power loss. Those are the four efficiency factors that will be analyzed in this chapter.

3.1 Redistribution Power loss

Redistribution power loss occurs when two capacitors with different charges are connected together. Let's consider a scenario with two capacitors Cp and Cout as illustrated in figure 3.1. The initial charge of its capacitor is

$$E_{initial} = \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2 \tag{3.2}$$

In the charge phase, Cp is charged to V_{in}. During the pump phase, the voltage at the top plate of Cp is $2V_{in}$ however V_{out} is lower than $2V_{in}$ due to I_{out} constantly discharging the capacitor C_{out}. As a result, the final energy at the output is characterized as 3.3

$$E_{final} = \frac{1}{2}(C_1 + C_2)V_{final}^2 \tag{3.3}$$

The redistribution loss E_{loss} is the difference between the initial and final energy.

$$E_{loss} = E_{initial} - E_{final} = \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2 - \frac{1}{2}(C_1 + C_2)V_{final}^2 \tag{3.4}$$

However, due to Kirchhoff's charge law (KQL), the total sum of all charges leaving a node is equal to zero as a result

$$Q_{inital} = Q_{final} \tag{3.5}$$

The charge of its capacitor is given by the equation 3.6

$$Q = C * V \tag{3.6}$$

When substituting the equations 3.5 and 3.7

$$C_1V_1 = (C_1 + C_2)V_{final} \tag{3.7}$$

Solving for V_{final} we get

$$V_{final} = \frac{C_1V_1 + C_2V_2}{(C_1 + C_2)} = \frac{C_pV_{in} + C_{out}V_{out}}{(C_{in} + C_{out})} \tag{3.8}$$

However, once C_{out} is charged to V_{out2} it is then discharged by I_{out} to V_{out1} over one switching cycle thus the redistribution power loss can be calculated by multiplying the energy loss with the switching frequency. Hence the total power loss is illustrated in the following equation

$$P_{loss} = E_{initial} * f_{switching} = \frac{1}{2}f_s(C_pV_{in}^2 + C_{out}V_{out1}^2 - C_p(V_{out2} - V_{out1})^2 - C_{out}V_{out2}^2) \tag{3.9}$$

It is apparent that the redistribution power loss depends on the size of the two capacitors and the switching frequency f_s of the circuit.

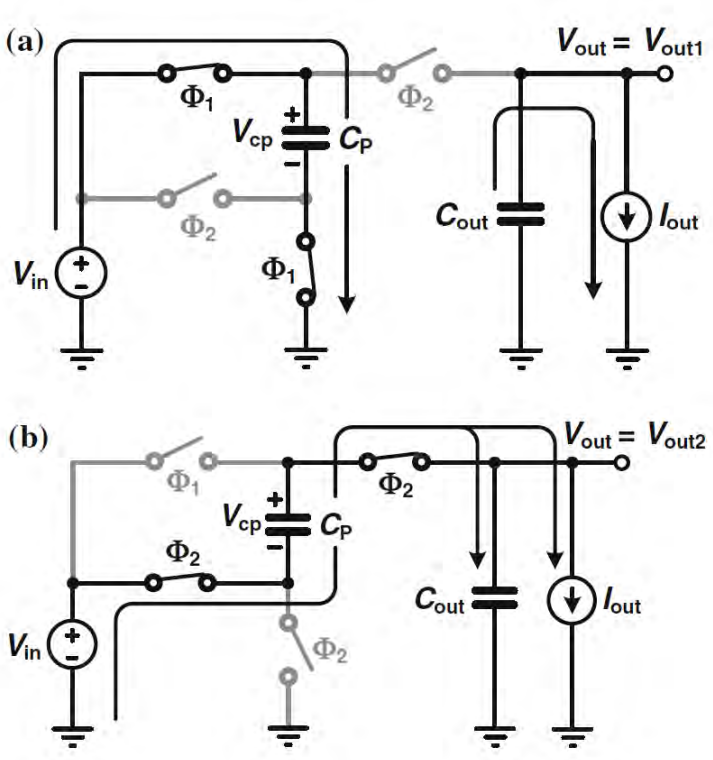

Figure 3.1: Redistribution in (a)Charge phase (b) pump phase [1]

3.2 Conduction Power Loss

The two main components when designing a charge pump are the capacitors and the switches. Ideally, switches operate with a zero r_{on} resistance. However, in most applications switches are designed using MOSFETs with an internal resistance significant enough to be the main reason for the conduction losses. Capacitors also contribute to the conduction loss with their parasitic equivalent series resistance (ESR), but those losses are negligible compared to the losses produced by the MOSFET's resistance. When MOSFETs operate in the linear region they act as a voltage-controlled resistor with a current path from the drain to the source this resistance is calculated by 3.10

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{gs} - Vth)} \tag{3.10}$$

Where μ is the mobility of the holes or electrons for pmos and nmos respectively. C_{ox} is the gate-oxide capacitance. W and L are the transistor's width and length respectively. Finally, V_{gs} is the voltage between the gate and the source of the transistors, and V_{th} is the threshold voltage. Hence with constant transistor sizes and drain current the conduction loss is equal to

$$P_{loss} = \frac{I_D^2 D}{\mu C_{ox} \frac{W}{L}(V_{gs} - Vth)} \tag{3.11}$$

where I_D is the drain current and D is the duty cycle of the circuit. It is clear that the conduction losses of the circuit are reduced by increasing the width and decreasing the length of the transistors.

3.3 Switching Power Loss

If the length of a transistor is constant increasing the width is a good strategy to decrease the conduction losses of the circuit. However, increasing the width also increases the parasitic capacitance of the transistor resulting in switching power loss. Switching power loss occurs when charging and discharging those parasitic capacitors. As shown in figure 3.2 parasitic capacitors appear in all the terminals of the transistor. However, the gate-source capacitor is the larger contributor when talking about the switching power loss as shown in the following equation.

$$P_{loss,C_{gs}} = f_s C_{ox} \sum_i W_i L_i V_{gs,i}^2 \tag{3.12}$$

Where W and L are the width and length of the transistor and $V_{gs,i}^2$ is the voltage between the gate and source of the transistor i. As equation 3.12 the switching loss is directly proportional to the product of W and L. Hence, to minimize both the switch and conductive loss, there is an optimal value for the width of the transistor depending on the design and on the technology of the transistors.

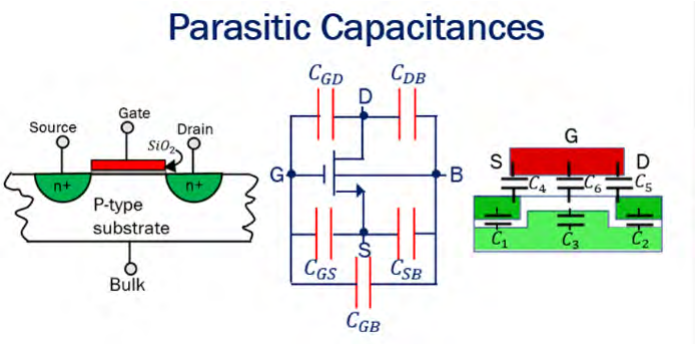

Figure 3.2: Parasitic capacitances in a MOSFET transistor [2]

3.4 Reversion Power Loss

Although the cross-coupled charge pump does not suffer from voltage drops due to the transistors' threshold, it suffers from reversion power losses. Let's consider the basic cross-coupled circuit illustrated in Figure 3.3 this topology suffers from several intrinsic loss paths, namely output, pumping, and short-circuit losses. Pumping loss occurs on the rising edge of CLK where NMOS NM1 is not totally off and charge from C1 is transferred back to the input through MN1. During the falling edge of CLK output loss occurs and charge flows through MP1 back to C1. During the transition between the clocks for a brief moment, both MN1 and MP1 are on thus charge flow from the input back to the output degrading the efficiency massively. In order to solve the short circuit loss the circuit must implement non-overlapping clocks in order to avoid this huge efficiency loss.

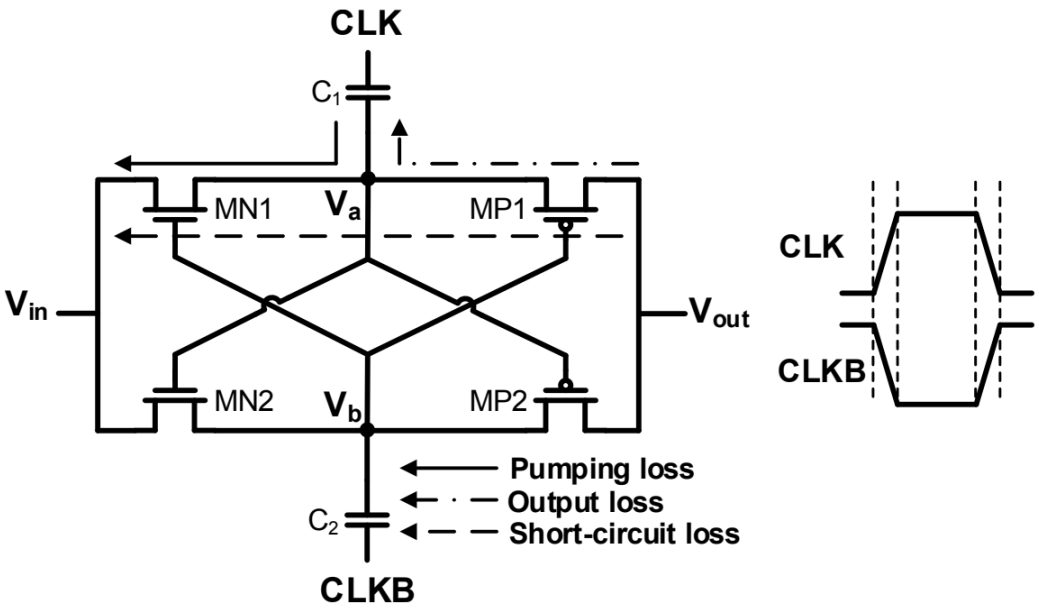

Figure 3.3: Reversion losses in cross-coupled charge pumps [3]

Chapter 4

The Proposed Cross-Coupled Fractional Buck-Boost converter

The previous chapters focused on the most popular charge pump topologies and the mechanisms of power loss in switched capacitor circuits. This case study presents a novel fractional cross-coupled charge pump aiming at reducing die area while providing an efficient and stable power source for multiple sub-circuits of an electronic system. This chapter starts with an analysis of the necessary capacitor topologies required to achieve the voltage fractions and continues with the design of the main circuit.

4.1 The Proposed Capacitor topologies

4.1.1 1/3 Cross-Coupled Charge Pump

In order to obtain the necessary fractions the proposed circuit employs the main cross-coupled design with the addition of a capacitor, a driver, and a control transistor (N2) on each rail. The $\frac{1}{3}$ fraction is achieved by connecting the flying capacitor and the output capacitor in series in the charge stage and in parallel in the discharge stage 4.1. During the charge stage CLK and Clk' are high and low respectively, the transistors N1 and N2 remain in the off state while P1 is turned on. Consequently, the top plate of capacitor Cf1 is connected to Vin and its bottom plate is linked to Cf2 through its driver. This, in turn, connects Cf2's bottom plate to the output via its driver placing all the capacitors in a series configuration. In the discharge stage Clk is low and Clk' is high this triggers the activation of the transistors N2 and N3 while

P1 is off. As a result, both top plates of Cf1 and Cf2 are connected to the output via N1 and N2, and their bottom plates are connected to ground through their respective drivers resulting in the required parallel connection. The voltage of the capacitors on each stage can be seen in the following equations 4.1 4.2. Figure 4.1 depicts only one rail of the cross-coupled charge pump however the working principle and the equations remain the same for the opposite rail.

$$Charge:$$

$$\begin{aligned} V_{Cf1} &= V_{in} - V_2 \\ V_{Cf2} &= V_2 - V_{out} \end{aligned} \tag{4.1}$$

$$Discharge:$$

$$\begin{aligned} V_{out} &= V_{Cf1} + V_{Cf2} \\ 2V_{out} &= V_{in} + V_2 - V_2 + V_{out} \\ 2V_{out} &= V_{in} - V_{out} => V_{out} = \frac{1}{3}V_{in} \end{aligned} \tag{4.2}$$

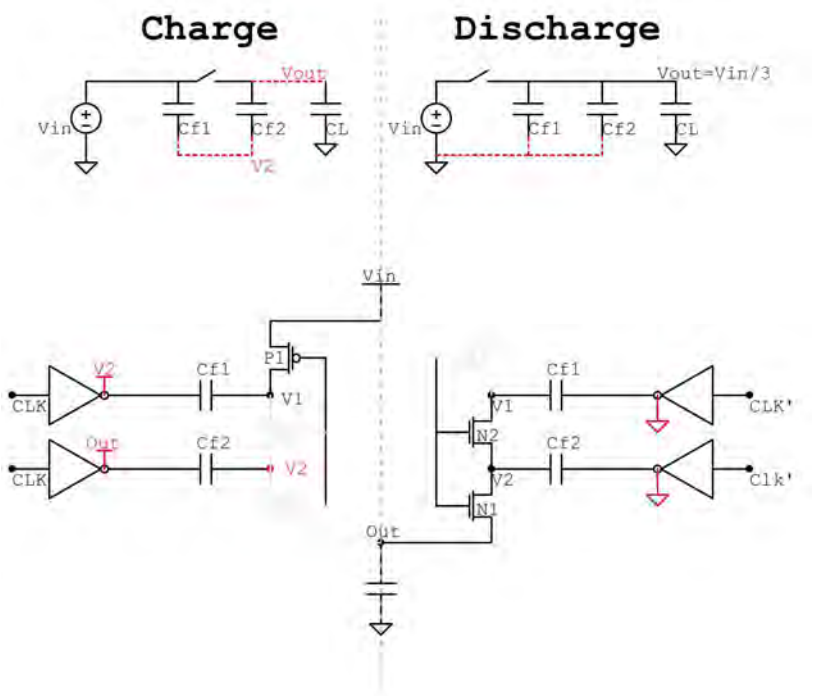

Figure 4.1: 1/3 Cross-Coupled Charge Pump

4.1.2 1/2 Cross-Coupled Charge Pump

The main challenge when designing the 1/2 Charge Pump topology is the elimination of one flying capacitor. As shown in figure 4.2 during the charge stage Cf1 is effectively

short-circuited and the flying capacitor Cf2 is connected in series with the output capacitor. In the discharge stage, Cf1 is entirely disconnected from the circuit while Cf2 is connected in parallel with the output capacitor. This is achieved by replacing the NMOS with a PMOS (P2) as a control transistor. As mentioned before during the charge stage both P1 and P2 are active thus Cf1 is short-circuited and Cf2's top plate is connected to Vin while its bottom plate is linked through its driver to the output capacitor. During the discharge stage CLK' is high and Clk is low resulting in the activation of N1 and the deactivation of P1 and P2 as a result the output capacitor is connected to Cf2's top plate via N1 while Cf2's bottom plate is grounded through its driver establishing the required parallel connection. It's important to note that the only difference between the 1/2 and the 1/3 topologies is the replacement of the control transistor and the drives remain the same.

$$Charge : V_{Cf1} = V_{in} - V_{out} \tag{4.3}$$

$$Discharge : V_{out} = V_{Cf1} => V_{out} = \frac{1}{2}V_{in} \tag{4.4}$$

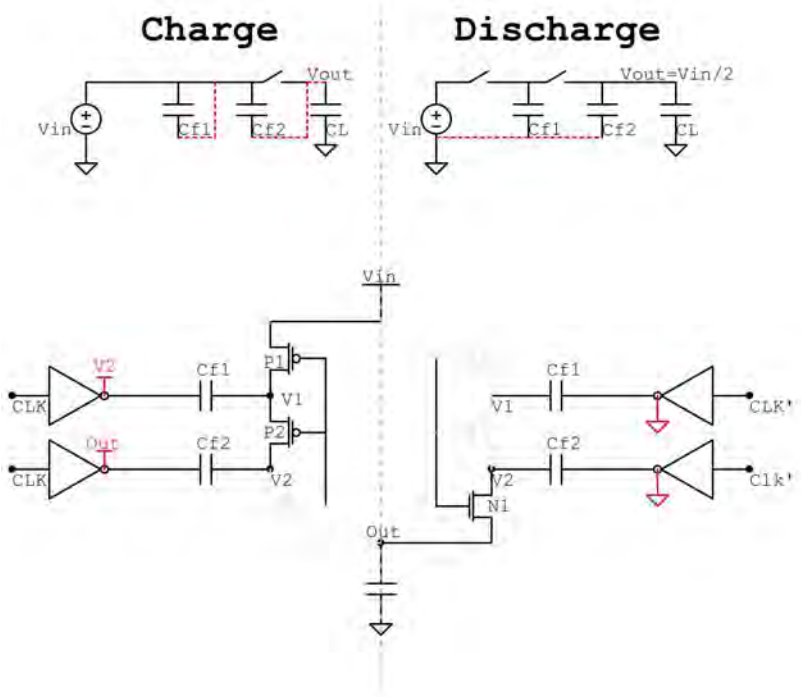

Figure 4.2: 1/2 Cross-Coupled Charge Pump

4.1.3 2/3 Cross-Coupled Charge Pump

The 2/3 topology retains the control Pmos and the sole difference with the 1/2 topology is the capacitor drivers. During the charge stage, CLK is high and CLK' is low thus the Pmos transistors P1 and P2 are activated connecting the top plates of both Cf1 and Cf2 to Vin while their bottom plates are linked to the output capacitor through the drivers. This configuration establishes the parallel connection between Cf1 and Cf2 and connects their parallel combination with the output capacitor. During the discharge stage the clocks swift making CLK low and CLK' high activating the Nmos transistor N1 while shutting down both pmos transistors P1 and P2. This results in the output capacitor getting connected with the top plate of Cf2 via N1 while Cf2's driver connects its bottom plate with the top plate of Cf1 resulting in the series combination of the output and both flying capacitors as shown in Figure 4.3. Equation 4.5 shows that during the charge state, both capacitors are charged to $Vin - V_{out}$ and on the discharge state after establishing the series connection between the capacitors the output voltage reaches $\frac{2}{3}V_{in}$ 4.6.

$$Charge: \quad V_{Cf1} = V_{Cf2} = V_{in} - V_{out} \tag{4.5}$$

$$Discharge: \quad V_{out} = V_{Cf1} + V_{Cf2} \quad V_{out} = 2V_{in} - 2V_{out} => V_{out} = \frac{2}{3}V_{in} \tag{4.6}$$

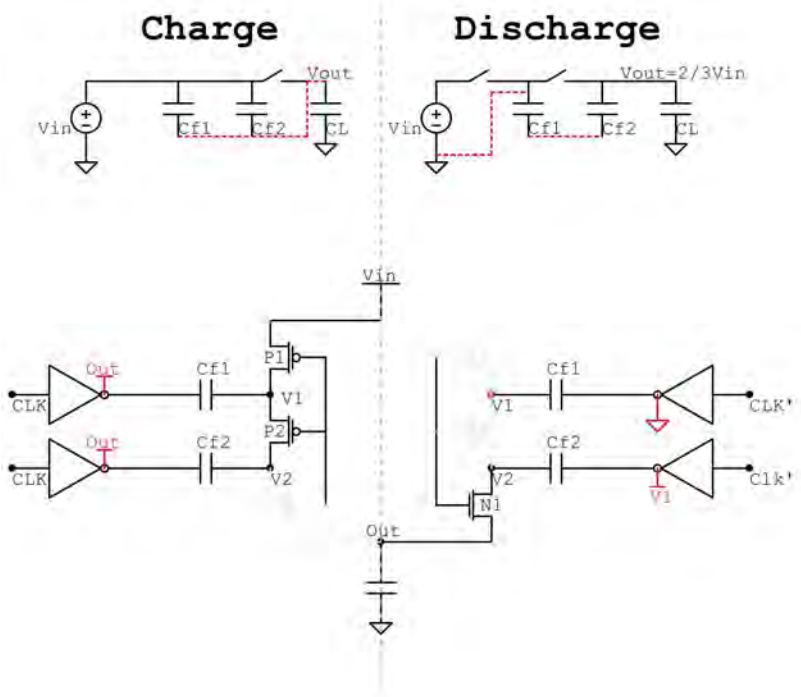

Figure 4.3: 2/3 Cross-Coupled Charge Pump

4.1.4 3/2 Cross-Coupled Charge Pump

The main advantage of the cross-coupled charge pump lies in the seamless transition between Buck and Boost modes by simply swapping the input and output terminal. As shown in figure 4.4 3/2 charge pump circuit layout mirrors that of the 2/3 charge pump with inverted input-output terminals. During the charge stage CLK is low and CLK' is high causing the NMOS transistor N1 to be active while disabling the PMOS transistors P1 and P2. During this stage, the flying capacitors Cf1 and Cf2 are connected in series with Cf2 connected to Vin through N1 and linked to Cf1 via its driver. Following the transition of the clock states where CLK goes high and CLK' goes low, the circuit enters the discharge stage. In this phase, both the flying capacitors and the output capacitor are connected in parallel with the bottom plates of the flying capacitors connected to Vin through their drivers. As indicated by the following equations, during the charge stage The capacitor Cf2 is charged to $V_{in} - V_{Cf2}$ 4.7. However, during the discharge phase, with the capacitor drivers connected to Vin, the output value is equal to 4.8.Replacing V_{Cf2} from 4.7 to 4.8 results in 4.9. Finally by adding 4.8 and 4.9 results in 4.10 indicating the output voltage is indeed $\frac{3}{2}V_{in}$.

$$Charge: \quad V_{Cf2} = V_{in} - V_{Cf1} \tag{4.7}$$

$$Discharge:$$

$$V_{out} = V_{Cf1} + V_{in} = V_{Cf2} + V_{in} \tag{4.8}$$

$$V_{out} = 2V_{in} - V_{Cf1} \tag{4.9}$$

$$2V_{out} = 3V_{in} => V_{out} = \frac{3}{2}V_{in} \tag{4.10}$$

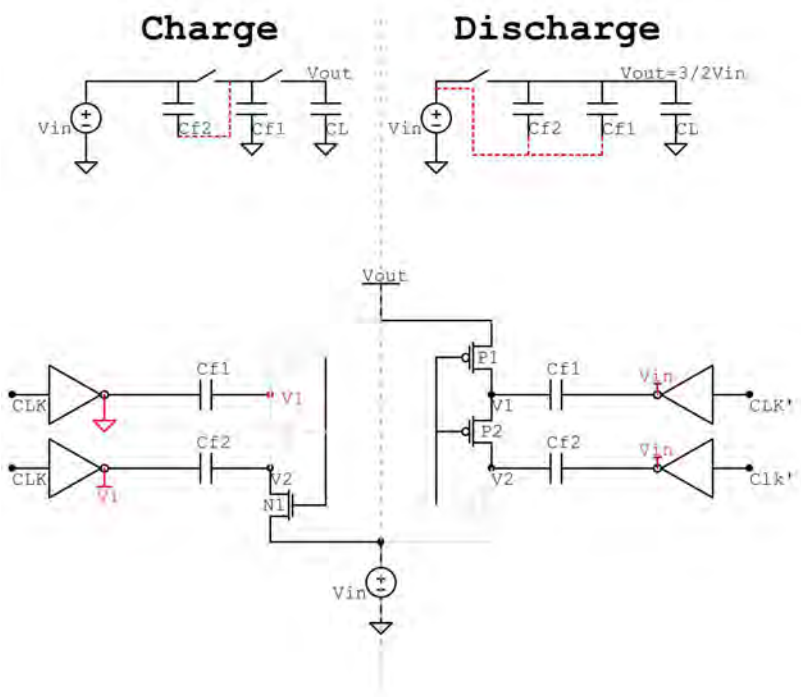

Figure 4.4: 3/2 Cross-Coupled Charge Pump

4.1.5 2/1 Cross-Coupled Charge Pump

As mentioned before the 2/1 topology mirrors the 1/2 topology with the inverted input output terminals. During the charge stage the flying capacitor Cf1 gets completely cut off by the deactivated transistors P1 and P2 while Cf2 is charged to Vin via N1. In the discharge stage the capacitor Cf1 gets short-circuited and Cf1 is connected in parallel with the output transistor while its bottom gets connected to Vin through the driver. As a result the output voltage reaches 2Vin.

$$Charge: V_{Cf2} = V_{in} \tag{4.11}$$

$$Discharge: V_{out} = V_{Cf2} + V_{out} => V_{out} = \frac{2}{1}V_{in} \tag{4.12}$$

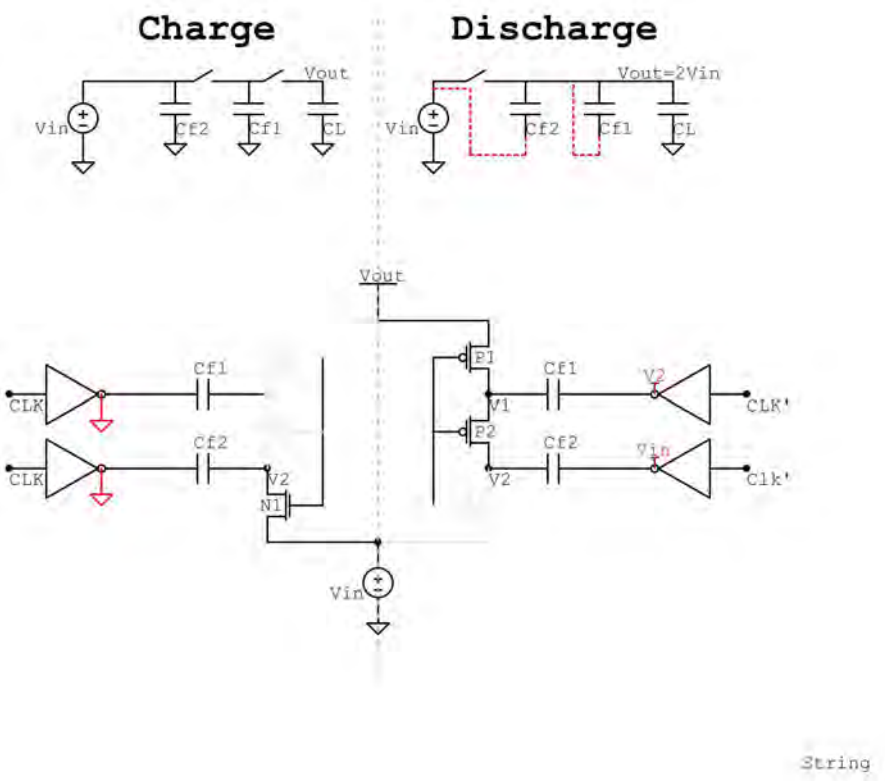

Figure 4.5: 2/1 Cross-Coupled Charge Pump

4.2 The Proposed Charge Pump Design

4.2.1 Charge Pump Core Circuit

The previous section analyzed the necessary methods of capacitor topology manipulation in order to obtain the fractions for the charge pump design. Moreover, it becomes clear that not every topology has the same control transistor and both PMOS and NMOS are necessary as the extra control transistor on each rail. This section presents the core circuit of the proposed charge pump. The transistors used in the previous section also known as the core control transistor are the NMOS (N1-N4) and the PMOS (P1-P4). The gate control signal for these transistors is internally generated and is connected in a cross configuration with Cf4 controlling the gates of N1, N3, and P1, P3 and Cf1 controlling the gates of N2, P2, and N4, P4. The transmission gates N5-N8 and P5-P8 are controlled by an internal select signal TSL4.1 and their purpose is to activate P3 and P4 when the signal is high while turning off N3 and N4, when TSL goes low N3 and N4 are turned on and P3 and P4 are deactivated enabling the necessary versatility in order to include multiple fractions. Furthermore, when a transmission gate is off the corresponding transistor enters a floating state. To prevent this,

transistors N9, and N10 ground the required NMOS gates while P9 and P10 provide the required PMOS gates with the circuit's highest voltage which can be either VDD for buck mode or Vout in boost mode essentially shutting down those transistors.

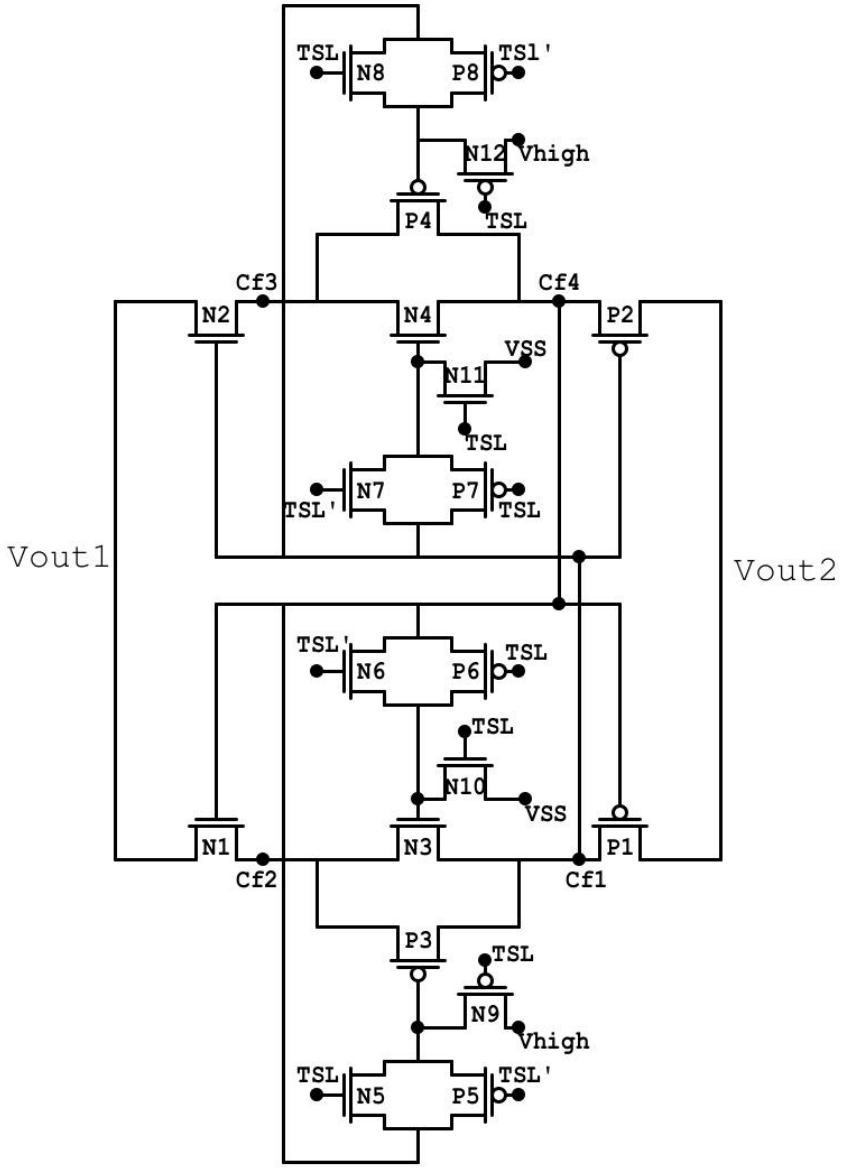

Figure 4.6: Charge Pump Core Circuit

4.2.2 Flying Capacitor Driver with Fraction select

Section 4.1 employed control transistor and capacitor drivers in order to provide multiple fractions, this section provides the design of the capacitor drivers. Figure 4.7 illustrates the drivers of Cf1 and Cf2, with Cf3 and Cf4 drivers following the same design logic. The capacitor drivers employ a select signal (Fsel) controlling transmission gate switches in order

to link the bottom plate of the flying capacitors to the selected fractional mode4.1 and a clock signal responsible for switching between the charge and discharge stage.

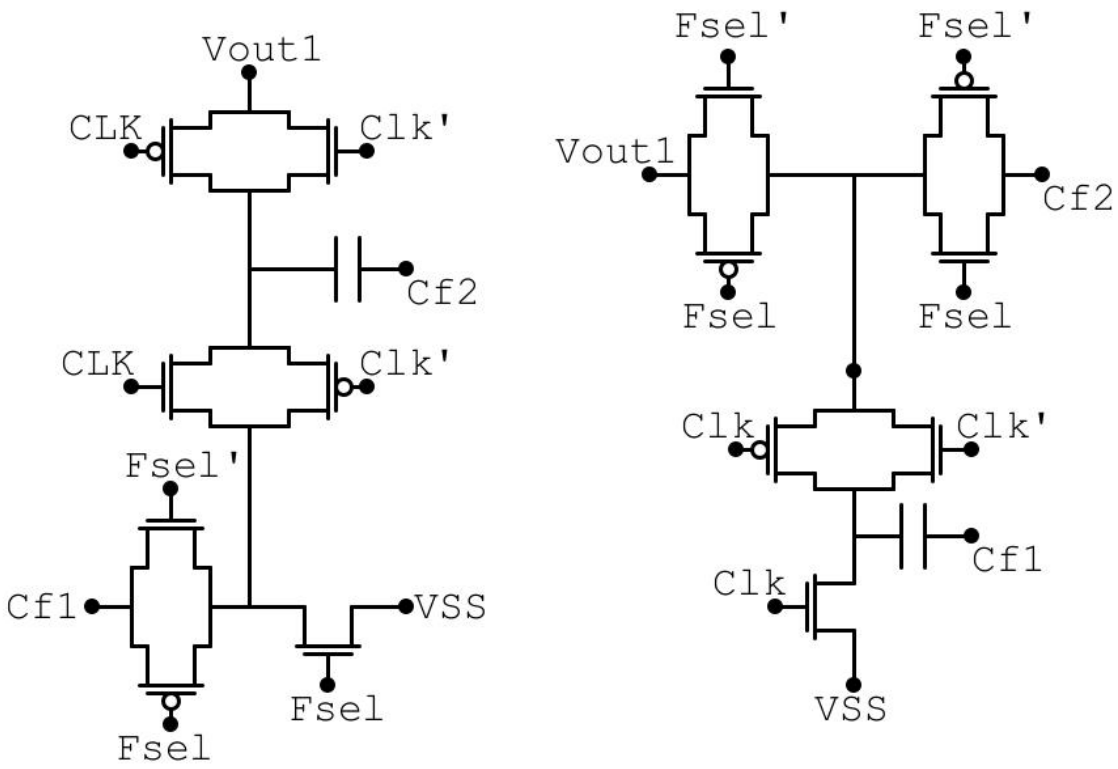

Figure 4.7: Flying Capacitor Driver with Fraction select

4.2.3 Buck-Boost selector

In the previous subsections, the signals Vout1 and Vout2 were introduced terminals. Those terminals undergo a swap between Vin and Vout with the aid of the Buck-Boost selector4.8. This circuit utilizes a control signal, denoted as SL, along with transmission gates to interchange those terminals, When SL is driven high, Vout1 is linked with Vout while Vout2 is connected to VDD. Conversely, when SL takes the value of VSS Vout1 gets connected to Vin while Vout2 is linked with the output terminal. This configuration plays a crucial role in meeting the specific requirements for the capacitor drivers necessitating a Vin connection in boost topologies and Vout connection on the Buck topologies.

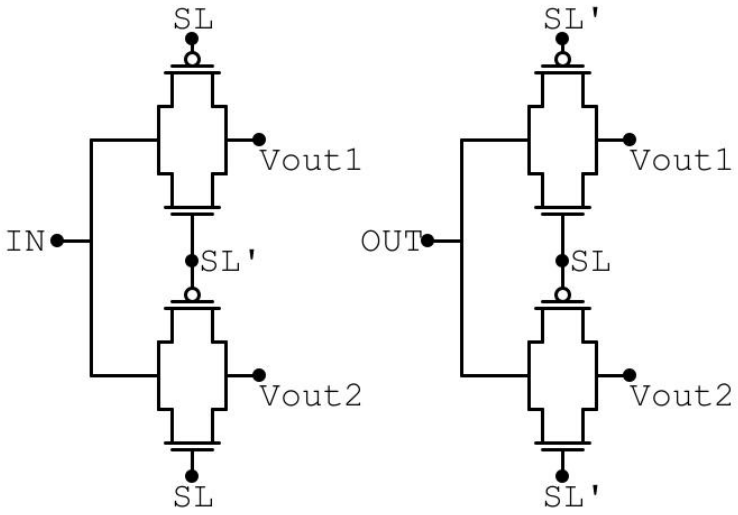

Figure 4.8: Buck-Boost selector

	TSL	SL	FSEL
1/3	HIGH	HIGH	HIGH
2/3	LOW	HIGH	LOW
1/2	LOW	HIGH	HIGH
3/2	LOW	LOW	LOW
2/1	LOW	LOW	HIGH

Table 4.1: Select signal values depending on the function

4.2.4 Adaptive PMOS Bulk bias circuit

When designing a CMOS circuit PMOS transistor must have their body at the circuit's highest potential. When operating at Buck mood PMOS's body is directly connected to Vin. The problems start to appear in Boost mode where Vout is higher than Vin when the steady has been reached but when the charge pump starts to operate Vin is still higher. In order to solve this an adaptive PMOS Bulk bias circuit has been employed consisting of two PMOS transistors4.9 providing constantly the circuit's highest voltage to the bulk of all PMOS transistors.

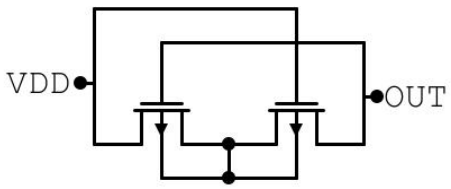

Figure 4.9: Adaptive PMOS Bulk bias circuit

Chapter 5

Simulation Results

The fractional output voltages of the charge pump are presented in Figure 5.1. Under low loads such as 150uA, it's clear that the output of the proposed charge pump reaches the expected values even when starting with zero volts as the initial condition. One of the most

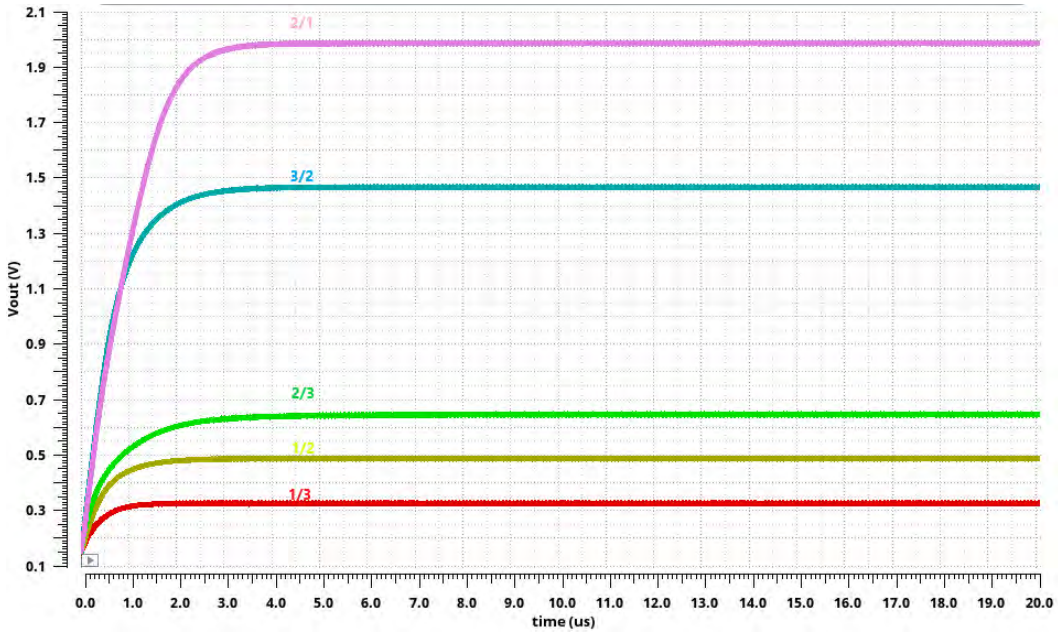

Figure 5.1: Fractional Output Voltage under 150uA load

important parameters when designing a charge pump is the output ripple. Figure 5.2 illustrates the output voltage values of a buck topology more specifically that of the 1/3 topology when stressed under different loads as well as its ripple. Figure 5.3 depicts the output voltages and the ripple effect in the 2/1 boost topology. Power efficiency is the most vital parameter in the design of a charge pump. Figure 5.4 illustrates the efficiency results of every topology of this design with the charge pump being calibrated for 1mA load. Table 5.1 presents the

parameters used on the design while table 5.2 illustrates the results under 1mA load for each topology.

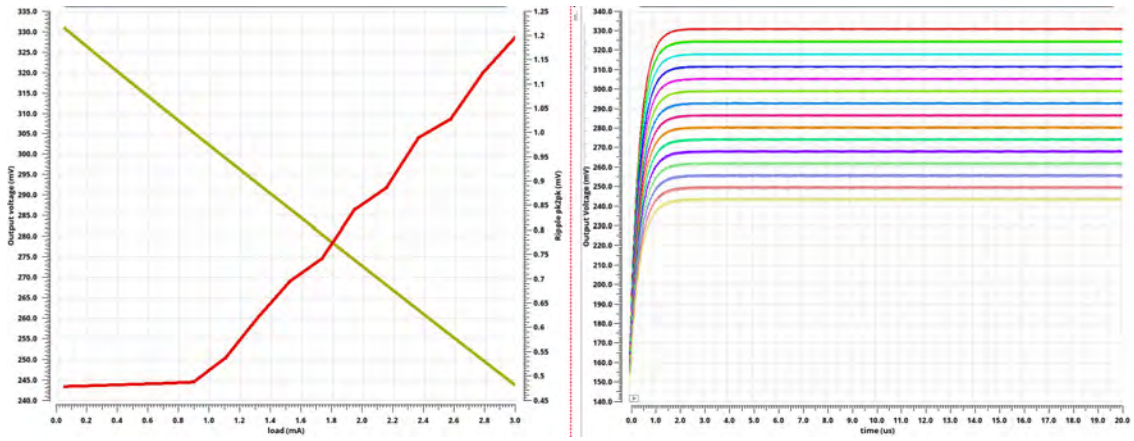

Figure 5.2: Output Voltage and ripple under different loads (50uA-3mA) in the 1/3 topology

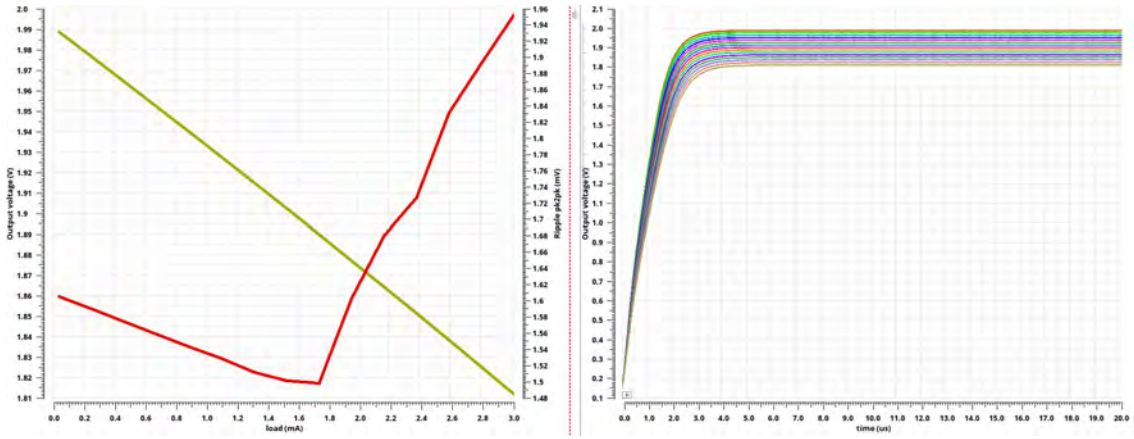

Figure 5.3: Output Voltage and ripple under different loads (50uA-3mA) in the 2/1 topology

	Technology	Frequency	Output Capacitor	Flying Capacitor	load	Input voltage
Parameters	IHP 0.13um	6.66Mhz	4nF	4x2nF	1mA	1V

Table 5.1: Parameter table

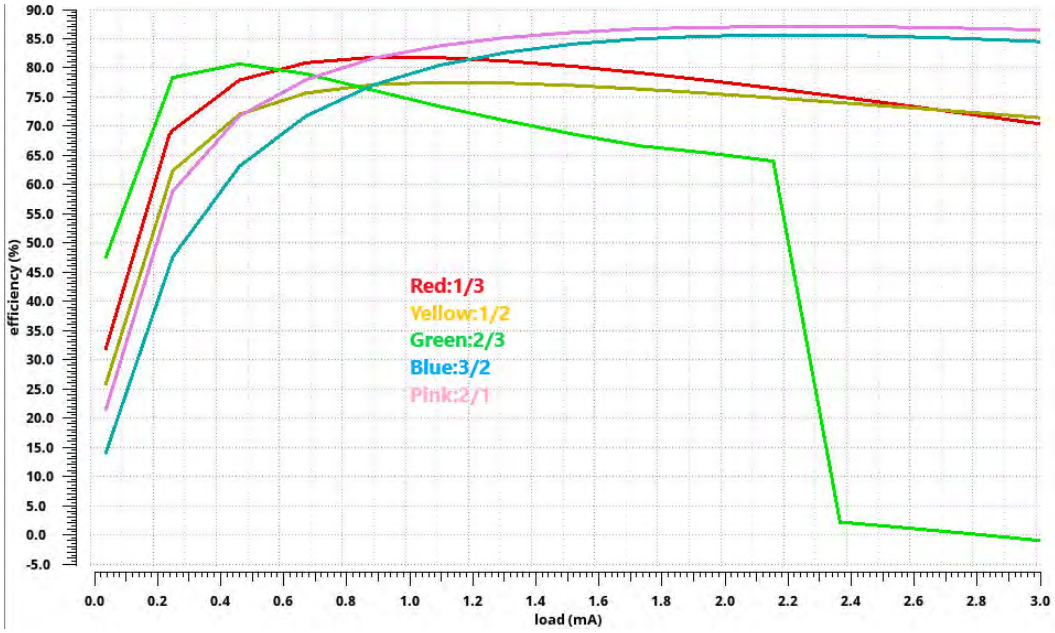

Figure 5.4: Efficiency Result

	Output Voltage	Ripple	Efficiency
1/3	302.1mV	507.9uV	81.87%
2/3	441.4mV	647.1uV	77.44%
1/2	523.1mV	728.4uV	74.76%
3/2	1.42V	752uV	78.97%
2/1	1.934V	1.536mV	82.87%

Table 5.2: Performance table

Chapter 6

Conclusion

This thesis presents a novel high-efficiency low ripple dual-mode fractional charge pump. Firstly the different capacitor topologies that compose the fractional charge pump were analyzed one by one. Furthermore, this thesis showcased how a cross-coupled charge pump can be turned into a fractional dual-mode Dc-Dc converter by the clever manipulation of control transistors, capacitor drivers, and the interchange of the input-output terminals. Moreover, its high performance in terms of high efficiency and low output voltage ripple for different loads is demonstrated by the presented simulations. The novelty of this thesis is the use of only one block to create a buck-boost fractional configuration reducing the required area on a chip while keeping a very high efficiency with low ripple. The circuit operation was verified using Cadence Virtuoso and designed with IHP's 0.13um transistor technology.

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